University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Discussion 4: Testbenches, CMOS, MIPS
Feb 19, 2010
Brandon Myers

1. Verilog Testbenches
   (a) useful functions: $display, $stop, $readmemb, $readmemh, $random
   (b) How do you generate a clock signal of 200MHz in your simulation?

   (c) Why is exhaustive testing of a 64-bit adder not possible?

2. Draw the CMOS implementation of Y=[D(AB+C)]'.

3. Draw the CMOS implementation of Y=[A(B+C)'+D].

4. (a) Draw a flipflop from inverters and transmission gates. Label all inputs and outputs.

   (b) Add synchronous set.
   (c) Add asynchronous set ("preset").

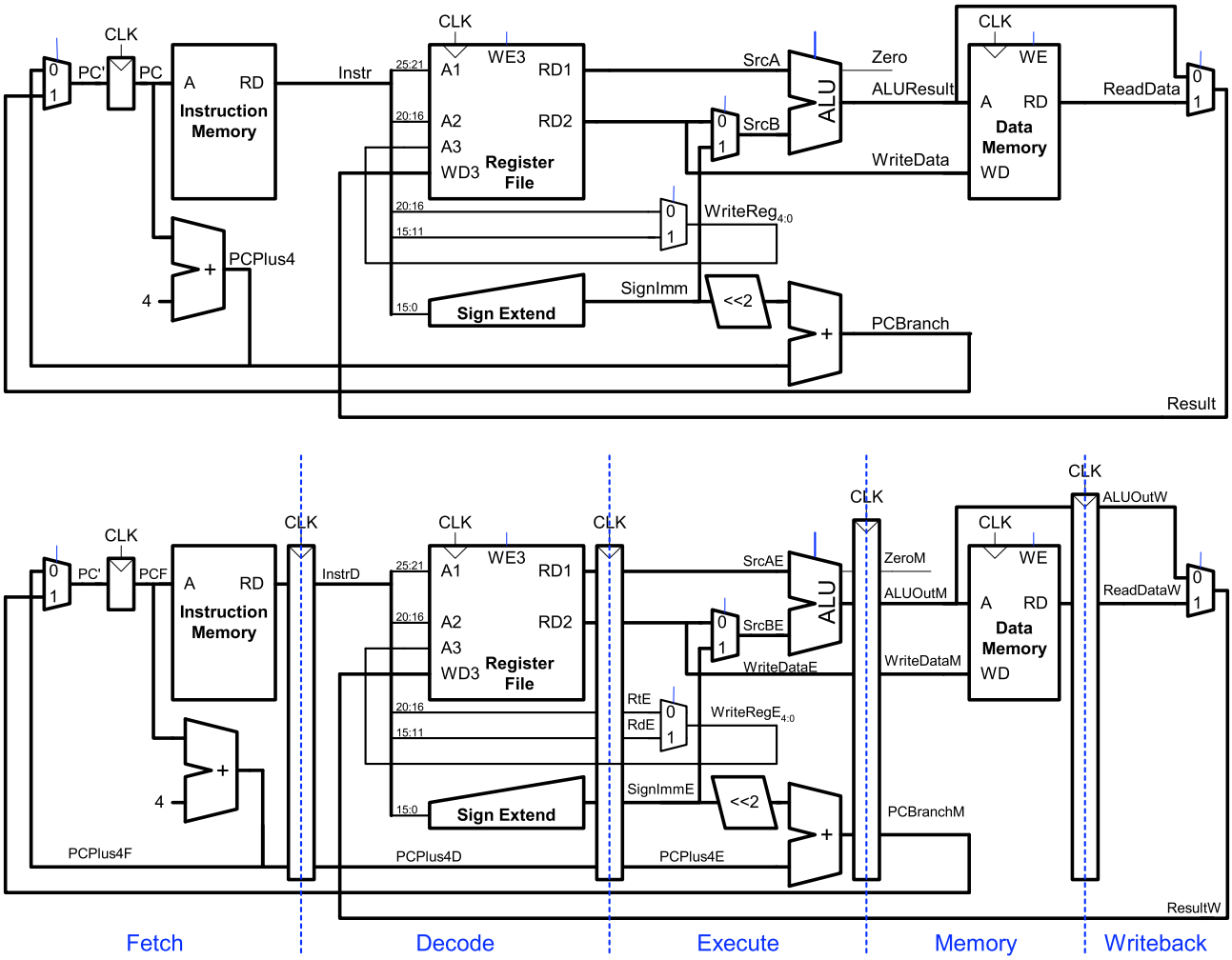
5. Implement the following instructions in the provided single-cycle and 5-stage processors. Add whatever hardware, wires, and control signals you need. Specify the values of all the control signals for each of the new instructions.

   (a) Jump-and-link-register (JALR) is a MIPS instruction, used to jump to an address stored in a register and save the PC+4 to the return address register $31. The RTL for this instruction is:

   ```
   code: jalr $rs;
   $31 <= PC+4;
   PC  <= R[rs];
   ```

   (b) Store-word-and-increment-immediate (SWInci) is a made up MIPS instruction, intended to optimize code that stores values to arrays. It is like a normal SW, except it also increments the register address by a given amount. The 16-bit immediate is shared: top 8 bits for the offset, the lower 8 bits to specify how much to increment the register address.

   ```
   code: swinci $rt, offset($rs), inc
   PC <= PC+4
   MEM[R[rs]+sign_ext(offset)] <= R[rt];
   R[rs] <= R[rs] + sign_ext(inc);
   ```



6. What is the metric used to evaluate performance of a processor? What are the product terms?

7. Suppose we have a 5-stage pipeline MIPS processor design. The delay through the logic of each stage is as follows: IF:2ns, ID:1ns, EX:1.8ns, MEM:2.8ns, WB:0.3ns.

   (a) What is the maximum clock frequency we can use for the processor?

   (b) How could we change the design to allow us to increase the clock frequency and still maintain correct functioning of the circuit?

   (c) What affect could your change have on the terms in the processor performance metric?

8. Suppose we added a complicated instruction (e.g. load-word-add) to the MIPS instruction set that could sometimes replace the occurence of 2 regular instructions (e.g. lw followed by add). How might this change affect each of the terms in the performance metric?