Sequential Logic Optimization

- State Minimization
- Algorithms for State Minimization
- State, Input, and Output Encodings
- Minimize the Next State and Output logic

Optimization in Context

- Understand the word specification
- Draw a picture
- Derive a state diagram and Symbolic State Table
- Determine an implementation approach (e.g., gate logic, ROM, FPGA, etc.)
- Perform STATE MINIMIZATION
- Perform STATE ASSIGNMENT
- Map Symbolic State Table to Encoded State Tables for implementation (INPUT and OUTPUT encodings)
- You can specify a specific state assignment in your Verilog code through parameter settings

Finite State Machine Optimization

- State Minimization
  - Fewer states require fewer state bits
  - Fewer bits require fewer logic equations
- Encodings: State, Inputs, Outputs
  - State encoding with fewer bits has fewer equations to implement
  - However, each may be more complex
  - State encoding with more bits (e.g., one-hot) has simpler equations
  - Complexity directly related to complexity of state diagram
  - Input/output encoding may or may not be under designer control

Algorithmic Approach to State Minimization

- Goal - identify and combine states that have equivalent behavior
- Equivalent States:
  - Same output
  - For all input combinations, states transition to same or equivalent states
- Algorithm Sketch
  - 1. Place all states in one set
  - 2. Initially partition set based on output behavior
  - 3. Successively partition resulting subsets based on next state transitions
  - 4. Repeat (3) until no further partitioning is required
  - states left in the same set are equivalent
  - Polynomial time procedure

State Minimization Example

- Sequence Detector for 010 or 110

<table>
<thead>
<tr>
<th>Input Sequence</th>
<th>Present State</th>
<th>Next State X=0</th>
<th>Next State X=1</th>
<th>Output X=0</th>
<th>Output X=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset 0</td>
<td>S0</td>
<td>S1</td>
<td>S2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>S3</td>
<td>S4</td>
<td>0 0</td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>S2</td>
<td>S5</td>
<td>S6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>S3</td>
<td>S0</td>
<td>S5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>S4</td>
<td>S0</td>
<td>S0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>S5</td>
<td>S0</td>
<td>S0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Method of Successive Partitions

<table>
<thead>
<tr>
<th>Input Sequence</th>
<th>Present State</th>
<th>Next State X=0</th>
<th>Next State X=1</th>
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<th>Output X=1</th>
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<tbody>
<tr>
<td>Reset</td>
<td>S0</td>
<td>S1</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>S1</td>
<td>S3</td>
<td>S4</td>
<td>0 0</td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>S2</td>
<td>S5</td>
<td>S6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>S3</td>
<td>S0</td>
<td>S5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>S4</td>
<td>S0</td>
<td>S0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>S5</td>
<td>S0</td>
<td>S0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

( S0 S1 S2 S3 S4 S5 S6 )
( S0 S1 S2 S5 S6 )
( S0 S2 S6 )
( S3 S5 S6 )
( S4 S6 )
( S4 S6 )

S1 is equivalent to S2
S3 is equivalent to S5
S4 is equivalent to S6
Minimized FSM

State minimized sequence detector for 010 or 110

<table>
<thead>
<tr>
<th>Input Sequence</th>
<th>Present State</th>
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<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
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<td>S2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>S2</td>
<td>S3</td>
<td>0</td>
</tr>
<tr>
<td>00</td>
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<td>S4</td>
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<tr>
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<td>0</td>
</tr>
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<td>10</td>
<td>S5</td>
<td>S6</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>S6</td>
<td>S7</td>
<td>0</td>
</tr>
<tr>
<td>000</td>
<td>S7</td>
<td>S8</td>
<td>1</td>
</tr>
<tr>
<td>001</td>
<td>S8</td>
<td>S9</td>
<td>0</td>
</tr>
<tr>
<td>010</td>
<td>S9</td>
<td>S10</td>
<td>0</td>
</tr>
<tr>
<td>100</td>
<td>S10</td>
<td>S11</td>
<td>0</td>
</tr>
<tr>
<td>101</td>
<td>S11</td>
<td>S12</td>
<td>1</td>
</tr>
<tr>
<td>110</td>
<td>S12</td>
<td>S13</td>
<td>0</td>
</tr>
<tr>
<td>111</td>
<td>S13</td>
<td>S14</td>
<td>0</td>
</tr>
</tbody>
</table>

7 States reduced to 4 States
3 bit encoding replaced by 2 bit encoding

Another Example

4-Bit Sequence Detector: output 1 after each 4-bit input sequence consisting of the binary strings 0110 or 1010

Final Reduced State Machine

15 states (min 4 FFs) reduced to 7 states (min 3 FFs)
More Complex State Minimization

- Multiple input example

inputs here

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<tr>
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<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>S1</td>
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<td>S3</td>
</tr>
<tr>
<td>S2</td>
<td>S3</td>
<td>S4</td>
</tr>
<tr>
<td>S3</td>
<td>S4</td>
<td>S5</td>
</tr>
<tr>
<td>S4</td>
<td>S5</td>
<td>S0</td>
</tr>
<tr>
<td>S5</td>
<td>S0</td>
<td>S1</td>
</tr>
</tbody>
</table>

symbolic state transition table

Minimized FSM

- Implication Chart Method
  - Cross out incompatible states based on outputs
  - Then cross out more cells if indexed chart entries are already crossed out

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
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</tr>
<tr>
<td>S2</td>
<td>S3</td>
<td>S4</td>
</tr>
<tr>
<td>S3</td>
<td>S4</td>
<td>S5</td>
</tr>
<tr>
<td>S4</td>
<td>S5</td>
<td>S0</td>
</tr>
<tr>
<td>S5</td>
<td>S0</td>
<td>S1</td>
</tr>
</tbody>
</table>

Minimizing Incompletely Specified FSMs

- Equivalence of states is transitive when machine is fully specified
- But it is not transitive when don't cares are present
  - e.g., state output
    - S0 - 0
    - S1 - 1
    - S2 - 1
- No polynomial time algorithm exists for determining best grouping of states into equivalent sets that will yield the smallest number of final states

Minimizing States May Not Yield Best Circuit

- Example: edge detector - outputs 1 when last two input changes from 0 to 1

<table>
<thead>
<tr>
<th>X</th>
<th>Q0</th>
<th>Q1</th>
<th>Q0'</th>
<th>Q1'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Q0' = X (Q0 xor Q1)
Q0'' = X Q0' Q1'

Another Implementation of Edge Detector

- "Ad hoc" solution - not minimal but cheap and fast

State Assignment

- Choose bit vectors to assign to each "symbolic" state
  - With n state bits for m states there are 2^m / (2^n - m)
  - 2^n codes possible for 1st state, 2^n-1 for 2nd, 2^n-2 for 3rd, ...
  - Huge number even for small values of n and m
  - Intractable for state machines of any size
  - Heuristics are necessary for practical solutions
  - Optimize some metric for the combinational logic
    - Size (amount of logic and number of FFs)
    - Speed (depth of logic and fanout)
    - Dependencies (decomposition)
State Assignment Strategies

- **Possible Strategies**
  - Sequential – just number states as they appear in the state table
  - Random – pick random codes
  - One-hot – use as many state bits as there are states (bit=1 → state)
  - Output – use outputs to help encode states
  - Heuristic – rules of thumb that seem to work in most cases
- **No guarantee of optimality – another intractable problem**

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One-hot State Assignment

- **Simple**
  - Easy to encode, debug
- **Small Logic Functions**
  - Each state function requires only predecessor state bits as input
- **Good for Programmable Devices**
  - Lots of flip-flops readily available
  - Simple functions with small support (signals dependent upon)
- **Impractical for Large Machines**
  - Too many states require too many flip-flops
  - Decompose FSMs into smaller pieces that can be one-hot encoded
- **Many Slight Variations to One-hot**
  - One-hot = all-0

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State Maps and Counting Bit Changes

**Bit Change Heuristic**

<table>
<thead>
<tr>
<th>State Name</th>
<th>Assignment</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>000</td>
<td>000</td>
</tr>
<tr>
<td>S1</td>
<td>011</td>
<td>111</td>
</tr>
<tr>
<td>S2</td>
<td>010</td>
<td>110</td>
</tr>
<tr>
<td>S3</td>
<td>001</td>
<td>011</td>
</tr>
</tbody>
</table>

Assignment: 00 01 11 10

**Adjacent Heuristics for State Assignment**

- **Adjacent codes to states that share a common next state**
  - Group 1’s in next state map
    - \( i, a, c, j \)
    - \( i, b, c, k \)
    - \( c = i \cdot a + i \cdot b \)

- **Adjacent codes to states that share a common ancestor state**
  - Group 1’s in next state map
    - \( i, a, b, j \)
    - \( k, a, c, J \)
    - \( b = i \cdot a \)
    - \( c = k \cdot a \)

- **Adjacent codes to states that have a common output behavior**
  - Group 1’s in output map
    - \( i, a, c, j \)
    - \( i, b, c, d \)
    - \( j = i \cdot a + i \cdot c \)
    - \( b = i \cdot a \)
    - \( d = i \cdot c \)

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Heuristics for State Assignment

**Successor/Predecessor Heuristics**

- High Priority: \( S_2 \) and \( S_4 \)
  - share common successor state \( S_5 \)
- Medium Priority: \( S_1 \) and \( S_4 \)
  - share common predecessor state \( S_3 \)
- Low Priority:
  - \( 0/1: S_0, S_1, S_2, S_3 \)
  - \( 0/1: S_0, S_1, S_2, S_3 \)

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Heuristics for State Assignment
Another Example

```
High Priority:   S'3, S'4   S'7, ...   S1, S2   2 x S'3, S'4   S'7, S'10
Low Priority:   0/0: S0, S1, S2, S'3, S'4, S'7   1/0: S0, S1, S2, S'3, S'4, S'7, S'10
```

Why Do These Heuristics Work?

- Attempt to maximize adjacent groupings of 1's in the next state and output functions
- Use outputs to help distinguish states
- Fits in nicely with synchronous Mealy implementations

Output-Based Encoding

- Reuse outputs as state bits - use outputs to help distinguish states
- Why create new functions for state bits when output can serve as well
- Works nicely with synchronous Mealy implementations

Choose assignment for S0 = 000

Place the high priority adjacency state pairs into the State Map

Repeat for the medium adjacency pairs

Repeat for any left over states, using the low priority scheme

Two alternative assignments at the left

General Approach to Heuristic State Assignment

- All current methods are variants of this
  1) Determine which states attract each other (weighted pairs)
  2) Generate constraints on codes (which should be in same cube)
  3) Place codes on Boolean cube so as to maximize constraints satisfied (weighted sum)

- Different weights make sense depending on whether we are optimizing for two-level or multi-level forms

- Can't consider all possible embeddings of state clusters in Boolean cube

Heuristics for ordering embedding

To prune search for best embedding

Expand cube (more state bits) to satisfy more constraints

Current State Assignment Approaches

- For tight encodings using close to the minimum number of state bits
- Best of 10 random seems to be adequate (averages as well as heuristics)
- Heuristic approaches are not even close to optimality
- Used in custom chip design

One-hot encoding

- Easy for small state machines
- Generates small equations with easy to estimate complexity
- Common in FP64s and other programable logic

Output-based encoding

- Ad-hoc - no tools
- Most common approach taken by human designers
- Yields very small circuits for most FSMs
Sequential Logic Implementation Summary

- Implementation of sequential logic
  - State minimization
  - State assignment

- Implications for programmable logic devices
  - When logic is expensive and FFs are scarce, optimization is highly desirable (e.g., gate logic, PLAs, etc.)
  - In Xilinix devices, logic is bountiful (4 and 5 variable TTS) and FFs are many (2 per CLB), so optimization is not so crucial an issue as in other forms of programmable logic.
  - This makes sparse encodings like One-Hot worth considering.