University of California at Berkeley
College of Engineering
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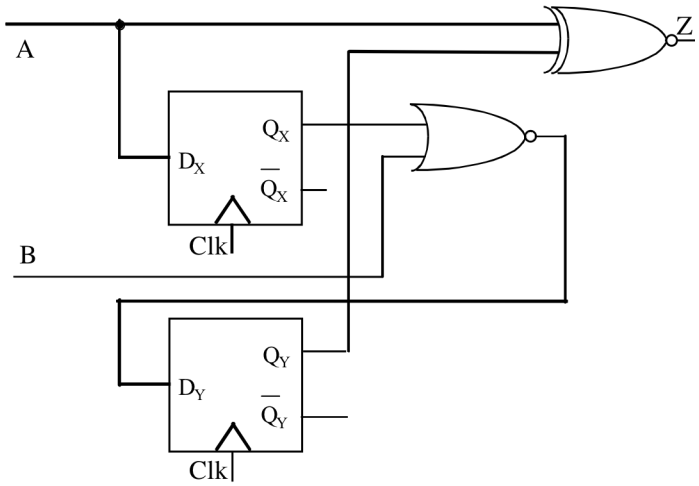
EECS 150 R. H. Katz
Spring 2007

Problem Set #4: Combinational and Sequential Logic
Assigned 6 February 2007, Due 16 February at 2 PM

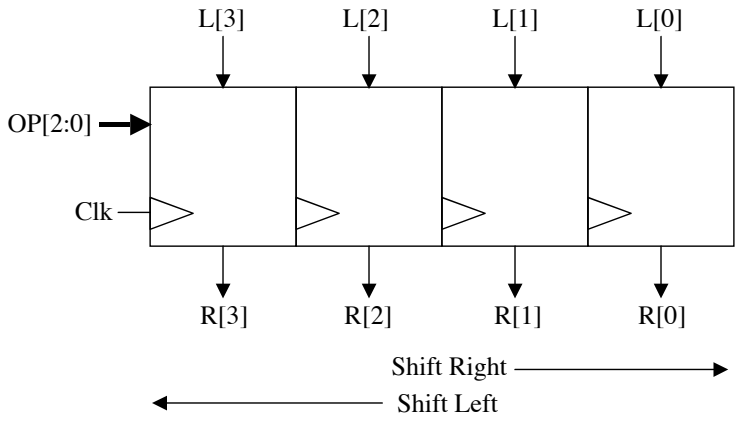
1. Given the following sequential logic circuit diagram:



(a) Is this a MEALY MACHINE or a MOORE MACHINE? Why?
(b) Write Boolean equations for the circuit nodes Z, D_x, and D_y.
(c) Write down the encoded state transition table.
(d) Write down the state transition diagram.

2. Write Verilog for a four-bit shifter subsystem to the following specification.

(a) The subsystem has four load inputs L[3:0], four register outputs R[3:0], a clock CLK, and a 3-bit operation input OP[2:0]. Here is a high-level block diagram:

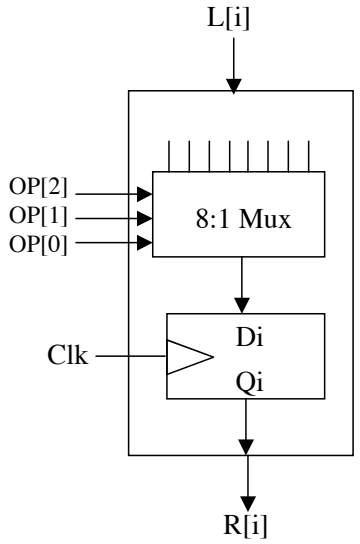


OP[2:0] is defined as:

000: Hold current value
001: Arithmetic shift right (shift right plus highest bit retains its value)
010: Arithmetic shift left (shift left plus lowest bit is filled with zero)
011: Circular shift right (shift right plus lowest bit wraps around to the highest bit)
100: Circular shift left (shift left plus highest bit wraps around to the lowest bit)
101: Logical shift right (shift right plus highest bit is filled with zero)
110: Reset register contents
111: Load register from inputs L[3:0]

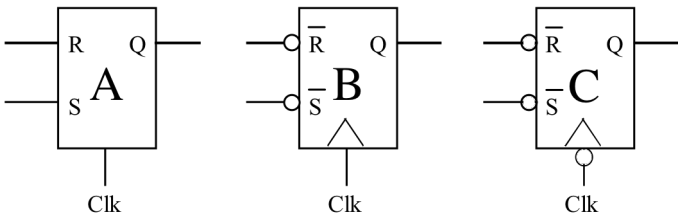
Write the system's description in high-level behavioral Verilog using a CASE statement and bit vector concatentions.

(b) Assume that the bit slice looks internally like this:



First write Verilog that describes the behavior of a single bit slice. Then write structural Verilog to describe how the multiplexer inputs should be wired for each of the four instances of the bit slice for i = 0, 1, 2, 3.

3. Device A is a clock-level sensitive R-S latch (i.e., it reacts to its inputs only when the clock is high). Device B is an $\overline{R}$-$\overline{S}$ "Flip-Flop" that is positive edge triggered. Device C is an $\overline{R}$-$\overline{S}$ "Flip-flop" that is negative edge triggered.



Assume 0 set-up and hold times, and 0 propagation delays. The devices B and C treat R and S as active low signals (i.e., Reset when $\overline{R}$ is zero and Set when $\overline{S}$ is zero). All are implemented using NAND gates. Initially they have 0 stored in them.

Complete the timing diagram below for the signals Q_A, Q_B, and Q_C, showing the behavior of the three different devices to the same R and S input changes (you can cut and past the following timing diagram into your homework):