First Midterm Exam—19 February 2004

- Topics to be covered:
  - Combinational logic design
    - From spec to truth table to K-map to Boolean Expression
      - Canonical forms of Boolean Expressions
      - Conversions of AND-OR logic to NAND or NOR logic
    - Two level logic implementations using gates, PLA, MUX, DEC, ROM, Xilinx CLB FPGA structures
      - Comparing implementation complexities/figures of merit
      - Combinational Verilog (lab expertise!)
  - Sequential logic design
    - Flip flop behavior, analysis, and timing diagrams
    - Using flip flops to design registers, shifters, counters
    - From spec to state diagram to Sequential Verilog
    - Amount of FSM implementation depends on how far into Lecture #7 we get on Tuesday

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- Exam mechanics
  - Worth ONLY 10% of course grade
  - In class, designed for 1 hour, full 80 minutes available
  - No Blue Book—all work to be done on the exam paper!
    - Bring pencil and eraser—DUMB to use pen!
    - Cheating = 0 on exam
      F in class plus letter to file for second offense
  - Closed Book, Closed Notes BUT
    - 8.5" x 11" two-sided crib sheet OK
      - Developing your crib sheet is a great way to study
      - Don't forget old exams and solutions are all on-line
    - No calculators, PDAs, laptops, icq to experts …
  - Write assumptions if problem spec is ambiguous
    - Difficult to ask questions during the exam itself
  - Written regrade appeals policy