Midterm II

- Tuesday, 30 March
- Lectures 8, 9, 10, 11, 12, 13; Lab Project Concept + Checkpoint #1; Verilog Specification and Simulation

Sequential Logic Implementation

- Models for representing sequential circuits
  - Abstraction of sequential elements
  - Finite state machines and their state diagrams
  - Inputs/outputs
  - Mealy, Moore, and synchronous Mealy machines
- Finite state machine design procedure
  - Deriving state diagram
  - Deriving state transition table
  - Determining next state and output functions
  - Implementing combinational logic

SDRAM Memory Controller

- Static RAM Technology
  - 6T Memory Cell
  - Memory Access Timing
- Dynamic RAM Technology
  - 1T Memory Cell
  - Memory Access Timing
- Detailed Memory System Timing (Lab Checkpoint #1)

Multimedia Network Switch Project

- Project Concept and Background
- Basic concept of a network router
- Streaming audio application
- Bells and Whistles

Computer Organization

- Computer design as an application of digital logic design procedures
- Computer = processing unit + memory system
- Processing unit = control + datapath
- Control = finite state machine
  - Inputs = machine instruction, datapath conditions
  - Outputs = register transfer control signals, ALU operation codes
  - Instruction interpretation = instruction fetch, decode, execute
- Datapath = functional units + registers
  - Functional units = ALU, multipliers, dividers, etc.
  - Registers = program counter, shifters, storage registers

State Machine Implementation

- Alternative controller FSM implementation approaches based on:
  - Classical Moore and Mealy machines
  - Time state: Divide and Counter
  - Jump counters
  - *Microprogramming (ROM) based approaches*
    - *branch sequencers*
    - *horizontal microcode*
    - *vertical microcode*