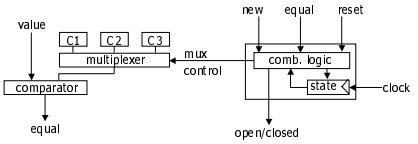
Sequential Logic

- Sequential Circuits
  - Simple circuits with feedback
  - Latches
  - Edge-triggered flip-flops
- Timing Methodologies
  - Cascading flip-flops for proper operation
  - Clock skew
- Basic Registers
  - Shift registers

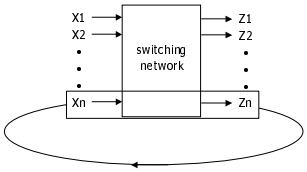
Sequential Circuits

- Circuits with Feedback
  - Outputs = f(inputs, past inputs, past outputs)
  - Basis for building "memory" into logic circuits
  - Door combination lock is an example of a sequential circuit
    - State is memory
    - State is an "output" and an "input" to combinational logic
    - Combination storage elements are also memory



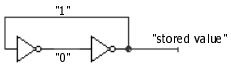
Circuits with Feedback

- How to control feedback?
  - What stops values from cycling around endlessly

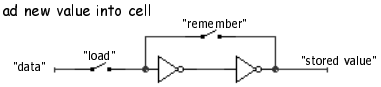


Simplest Circuits with Feedback

- Two inverters form a static memory cell
  - Will hold value as long as it has power applied

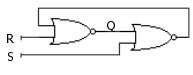


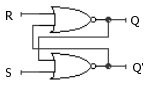
- How to get a new value into the memory cell?
  - Selectively break feedback path
  - Load new value into cell



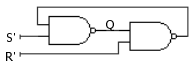
Memory with Cross-coupled Gates

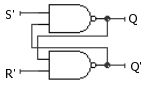
- Cross-coupled NOR gates
  - Similar to inverter pair, with capability to force output to 0 (reset=1) or 1 (set=1)



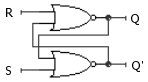


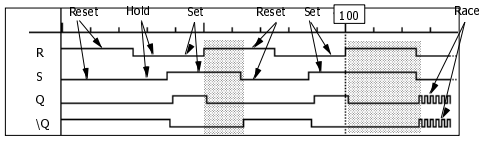
- Cross-coupled NAND gates
  - Similar to inverter pair, with capability to force output to 0 (reset=0) or 1 (set=0)





Timing Behavior

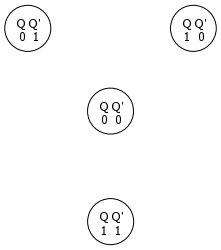




State Behavior of R-S latch

- Truth table of R-S latch behavior

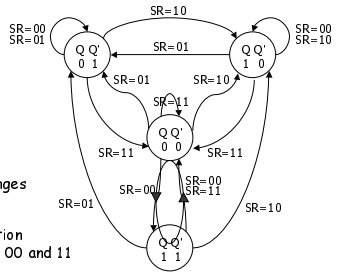
S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	unstable



Theoretical R-S Latch Behavior

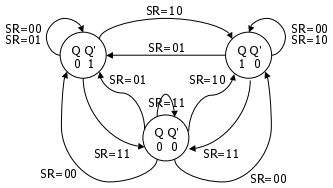
- State Diagram
  - States: possible values
  - Transitions: changes based on inputs

possible oscillation between states 00 and 11



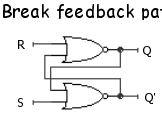
Observed R-S Latch Behavior

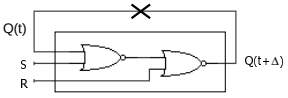
- Very difficult to observe R-S latch in the 1-1 state
  - One of R or S usually changes first
- Ambiguously returns to state 0-1 or 1-0
  - A so-called "race condition"
  - Or non-deterministic transition



R-S Latch Analysis

- Break feedback path





S	R	Q(t)	Q(t+Δ)	
0	0	0	0	hold
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	not allowed
1	1	1	X	

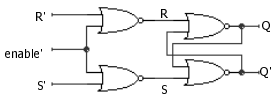
Q(t) \ S	0	0	X	1
0	0	0	X	1
1	1	0	X	1

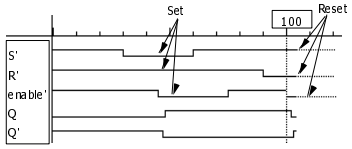
R

characteristic equation
$Q(t+\Delta) = S + R' Q(t)$

Gated R-S Latch

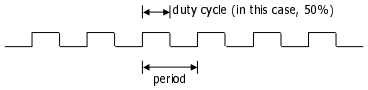
- Control when R and S inputs matter
  - Otherwise, the slightest glitch on R or S while enable is low could cause change in value stored





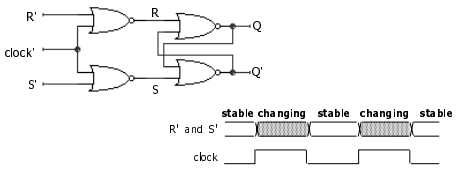
Clocks

- Used to keep time
  - Wait long enough for inputs (R' and S') to settle
  - Then allow to have effect on value stored
- Clocks are regular periodic signals
  - Period (time between ticks)
  - Duty-cycle (time clock is high between ticks - expressed as % of period)



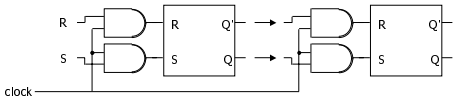
Clocks (cont'd)

- Controlling an R-S latch with a clock
  - Can't let R and S change while clock is active (allowing R and S to pass)
  - Only have half of clock period for signal changes to propagate
  - Signals must be stable for the other half of clock period



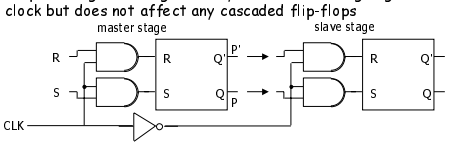
Cascading Latches

- Connect output of one latch to input of another
- How to stop changes from racing through chain?
  - Need to control flow of data from one latch to the next
  - Advance from one latch per clock period
  - Worry about logic between latches (arrows) that is too fast



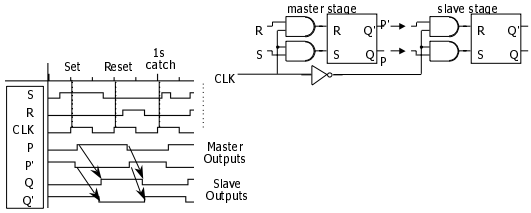
Master-Slave Structure

- Break flow by alternating clocks (like an air-lock)
  - Use positive clock to latch inputs into one R-S latch
  - Use negative clock to change outputs with another R-S latch
- View pair as one basic unit
  - master-slave flip-flop
  - twice as much logic
  - output changes a few gate delays after the falling edge of clock but does not affect any cascaded flip-flops



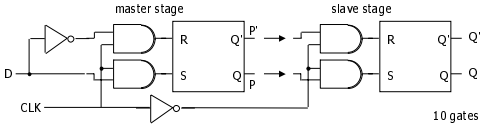
The 1s Catching Problem

- In first R-S stage of master-slave FF
  - 0-1-0 glitch on R or S while clock is high "caught" by master stage
  - Leads to constraints on logic to be hazard-free



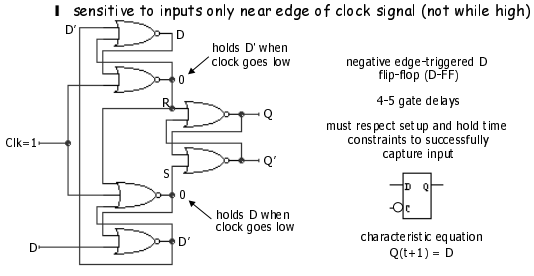
D Flip-Flop

- Make S and R complements of each other
  - Eliminates 1s catching problem
  - Can't just hold previous value (must have new value ready every clock period)
  - Value of D just before clock goes low is what is stored in flip-flop
  - Can make R-S flip-flop by adding logic to make D = S + R' Q



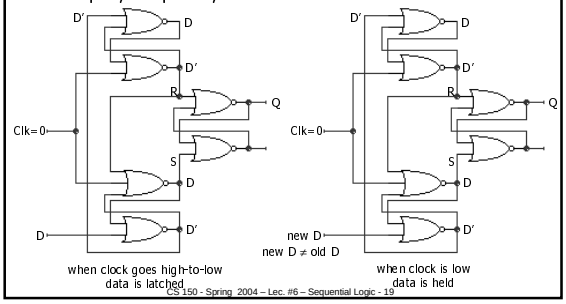
Edge-Triggered Flip-Flops

- More efficient solution: only 6 gates
  - sensitive to inputs only near edge of clock signal (not while high)



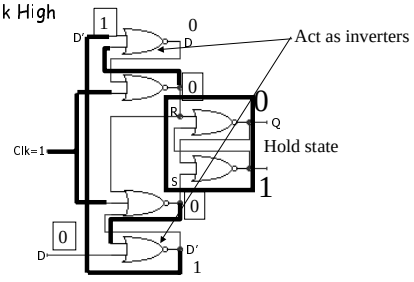
Edge-Triggered Flip-Flops (cont'd)

- Step-by-step analysis



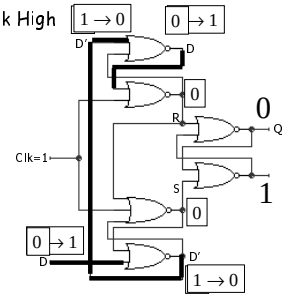
Edge-Triggered Flip-Flops (cont'd)

- D = 0, Clk High



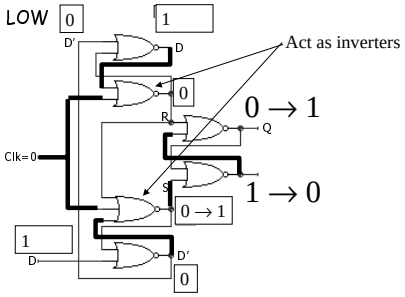
Edge-Triggered Flip-Flops (cont'd)

- D = 1, Clk High



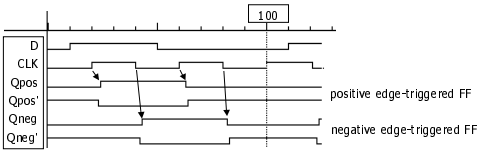
Edge-Triggered Flip-Flops (cont'd)

- D = 1, Clk LOW



Edge-Triggered Flip-Flops (cont'd)

- Positive edge-triggered
  - Inputs sampled on rising edge; outputs change after rising edge
- Negative edge-triggered flip-flops
  - Inputs sampled on falling edge; outputs change after falling edge



Negative Edge Trigger FF in Verilog

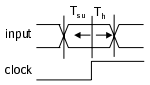
```
module d_ff (q, q_bar, data, clk);
  input  data, clk;
  output q, q_bar;
  reg    q;

  assign q_bar = ~q;

  always @(negedge clk)
    begin
      q <= data;
    end
endmodule
```

Timing Methodologies

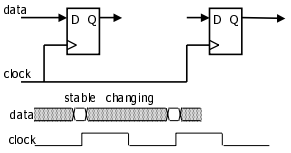
- Rules for interconnecting components and clocks
  - Guarantee proper operation of system when strictly followed
- Approach depends on building blocks used for memory elements
  - Focus on systems with edge-triggered flip-flops
    - Found in programmable logic devices
  - Many custom integrated circuits focus on level-sensitive latches
- Basic rules for correct timing:
  - (1) Correct inputs, with respect to time, are provided to the flip-flops
  - (2) No flip-flop changes state more than once per clocking event

Timing Methodologies (cont'd)

- Definition of terms
  - clock: periodic event, causes state of memory element to change; can be rising or falling edge, or high or low level
  - setup time: minimum time before the clocking event by which the input must be stable (Tsu)
  - hold time: minimum time after the clocking event until which the input must remain stable (Th)



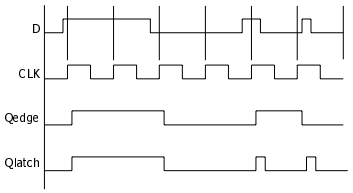
there is a timing "window" around the clocking event during which the input must remain stable and unchanged in order to be recognized



Comparison of Latches and Flip-Flops

positive edge-triggered flip-flop

transparent (level-sensitive) latch



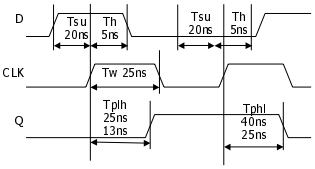
behavior is the same unless input changes while the clock is high

Comparison of Latches and Flip-Flops (cont'd)

Type	When inputs are sampled	When output is valid
unclocked latch	always	propagation delay from input change
level-sensitive latch	clock high (Tsu/Th around falling edge of clock)	propagation delay from input change or clock edge (whichever is later)
master-slave flip-flop	clock high (Tsu/Th around falling edge of clock)	propagation delay from falling edge of clock
negative edge-triggered flip-flop	clock hi-to-lo transition (Tsu/Th around falling edge of clock)	propagation delay from falling edge of clock

Typical Timing Specifications

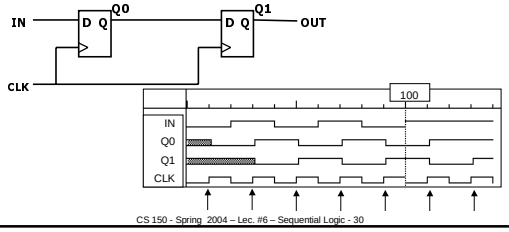
- Positive edge-triggered D flip-flop
  - Setup and hold times
  - Minimum clock width
  - Propagation delays (low to high, high to low, max and typical)



all measurements are made from the clocking event that is, the rising edge of the clock

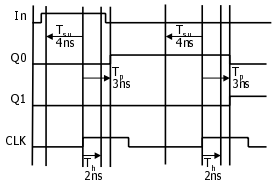
Cascading Edge-triggered Flip-Flops

- Shift register
  - New value goes into first stage
  - While previous value of first stage goes into second stage
  - Consider setup/hold/propagation delays (prop must be > hold)



Cascading Edge-triggered Flip-Flops (cont'd)

- Why this works
  - Propagation delays exceed hold times
  - Clock width constraint exceeds setup time
  - This guarantees following stage will latch current value before it changes to new value

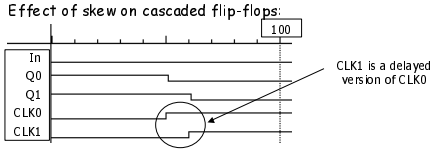


timing constraints guarantee proper operation of cascaded components

assumes infinitely fast distribution of the clock

Clock Skew

- The problem
  - Correct behavior assumes next state of all storage elements determined by all storage elements at the same time
  - This is difficult in high-performance systems because time for clock to arrive at flip-flop is comparable to delays through logic
  - Effect of skew on cascaded flip-flops:



original state: IN = 0, Q0 = 1, Q1 = 1
due to skew, next state becomes: Q0 = 0, Q1 = 0, and not Q0 = 0, Q1 = 1

Summary of Latches and Flip-Flops

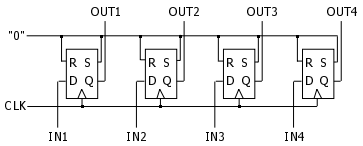
- Development of D-FF
  - Level-sensitive used in custom integrated circuits
    - can be made with 4 switches
  - Edge-triggered used in programmable logic devices
  - Good choice for data storage register
- Historically J-K FF was popular but now never used
  - Similar to R-S but with 1-1 being used to toggle output (complement state)
  - Good in days of TTL/SSI (more complex input function: D = JQ' + K'Q
  - Not a good choice for PALs/PLAs as it requires 2 inputs
  - Can always be implemented using D-FF
- Preset and clear inputs are highly desirable on flip-flops
  - Used at start-up or to reset system to a known state

Flip-Flop Features

- Reset (set state to 0) – R
  - Synchronous: Dnew = R' · Dold (when next clock edge arrives)
  - Asynchronous: doesn't wait for clock, quick but dangerous
- Preset or set (set state to 1) – S (or sometimes P)
  - Synchronous: Dnew = Dold + S (when next clock edge arrives)
  - Asynchronous: doesn't wait for clock, quick but dangerous
- Both reset and preset
  - Dnew = R' · Dold + S (set-dominant)
  - Dnew = R' · Dold + R'S (reset-dominant)
- Selective input capability (input enable/load) – LD or EN
  - Multiplexer at input: Dnew = LD' · Q + LD · Dold
  - Load may/may not override reset/set (usually R/S have priority)
- Complementary outputs – Q and Q'

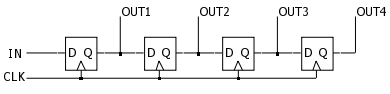
Registers

- Collections of flip-flops with similar controls and logic
  - Stored values somehow related (e.g., form binary value)
  - Share clock, reset, and set lines
  - Similar logic at each stage
- Examples
  - Shift registers
  - Counters



Shift Register

- Holds samples of input
  - Store last 4 input values in sequence
  - 4-bit shift register:



Shift Register Verilog

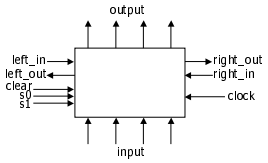
```
module shift_reg (out4, out3, out2, out1,  in, clk);
  output out4, out3, out2, out1;
  input  in, clk;
  reg    out4, out3, out2, out1;

always @(posedge clk)
  begin
    out4 <= out3;
    out3 <= out2;
    out2 <= out1;
    out1 <= in;
  end
endmodule
```


Shift Register Verilog

```
module shift_reg (out, in, clk);
  output [4:1] out;
  input  in, clk;
  reg    [4:1] out;

always @(posedge clk)
  begin
    out <= {out[3:1], in};
  end
endmodule
```


Universal Shift Register

- Holds 4 values
  - Serial or parallel inputs
  - Serial or parallel outputs
  - Permits shift left or right
  - Shift in new values from left or right



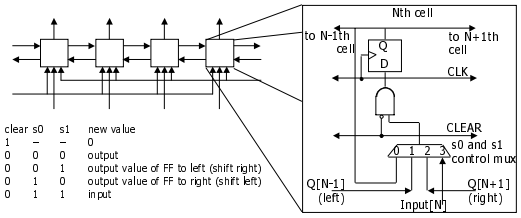
clear sets the register contents and output to 0

s1 and s0 determine the shift function

s0	s1	function
0	0	hold state
0	1	shift right
1	0	shift left
1	1	load new input

Design of Universal Shift Register

- Consider one of the four flip-flops
  - New value at next clock cycle:



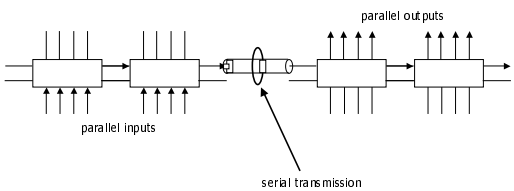
clear	s0	s1	new value
1	–	–	0
0	0	0	output
0	0	1	output value of FF to left (shift right)
0	1	0	output value of FF to right (shift left)
0	1	1	input

Universal Shift Register Verilog

```
module univ_shift (out, lo, ro, in, li, ri, s, clr, clk);
  output [3:0] out;
  output lo, ro;
  input  [3:0] in;
  input  [1:0] s;
  input  li, ri, clr, clk;
  reg    [3:0] out;

assign lo = out[3];
assign ro = out[0];

always @(posedge clk or clr)
  begin
    if (clr) out <= 0;
    else
      case (s)
      3: out <= in;
      2: out <= {out[2:0], ri};
      1: out <= {li, out[3:1]};
      0: out <= out;
    endcase
  end
endmodule
```

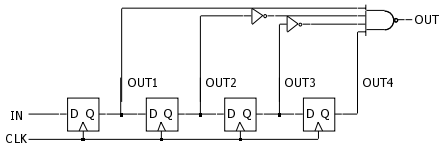

Shift Register Application

- Parallel-to-serial conversion for serial transmission



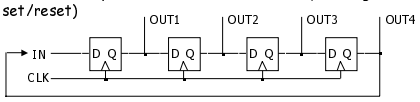
Pattern Recognizer

- Combinational function of input samples
  - In this case, recognizing the pattern 1001 on the single input signal

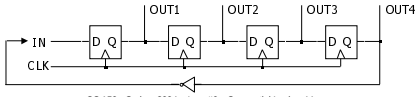


Counters

- Sequences through a fixed set of patterns
  - In this case, 1000, 0100, 0010, 0001
  - If one of the patterns is its initial state (by loading or set/reset)

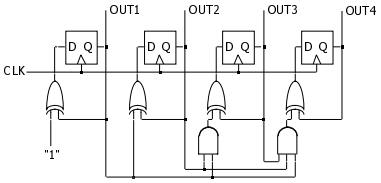


- Mobius (or Johnson) counter
  - In this case, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000



Binary Counter

- Logic between registers (not just multiplexer)
  - XOR decides when bit should be toggled
  - Always for low-order bit, only when first bit is true for second bit, and so on



Binary Counter Verilog

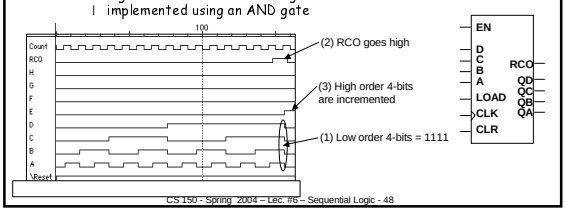
```
module shift_reg (out4, out3, out2, out1, clk);
  output out4, out3, out2, out1;
  input  in, clk;
  reg    out4, out3, out2, out1;

always @(posedge clk)
  begin
    out4 <= (out1 & out2 & out3) ^ out4;
    out3 <= (out1 & out2) ^ out3;
    out2 <= out1 ^ out2;
    out1 <= out1 ^ 1b'1;
  end
endmodule
```


Binary Counter Verilog

```
module shift_reg (out4, out3, out2, out1, clk);
  output [4:1] out;
  input  in, clk;
  reg    [4:1] out;

always @(posedge clk)
    out <= out + 1;

endmodule
```

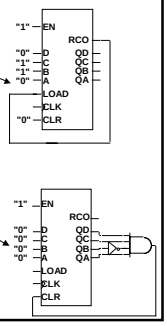

Four-bit Binary Synchronous Up-Counter

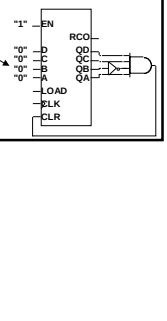
- Standard component with many applications
  - Positive edge-triggered FFs w/ sync load and clear inputs
  - Parallel load data from D, C, B, A
  - Enable inputs: must be asserted to enable counting
  - RCO: ripple-carry out used for cascading counters
    - high when counter is in its highest state 1111
    - implemented using an AND gate



Offset Counters

- Starting offset counters – use of synchronous load
  - e.g., 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1111, 0110, . . .
- Ending offset counter – comparator for ending value
  - e.g., 0000, 0001, 0010, ..., 1100, 1101, 0000
- Combinations of the above (start and stop value)





Sequential Logic Summary

- Fundamental building block of circuits with state
  - Latch and flip-flop
  - R-S latch, *R-S master/slave, D master/slave*, edge-triggered D FF
- Timing methodologies
  - Use of clocks
  - Cascaded FFs work because prop delays exceed hold times
  - Beware of clock skew
- Basic registers
  - Shift registers
  - Pattern detectors
  - Counters