EECS 150 Spring 2004

Lab Lecture 13
Project Checkoff & Report
4/23/2003

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Today

- Due Dates
- Checkoff procedures
- Testing Requirements
- A Brief Note about Broadcast
- The Project Report
- Project Grading

Due Dates

- Mon 4/26 @ 10am: Early Checkoff Files
- Mon 5/3 @ 10am: Checkoff Files
  - You may only submit *.V and *.EDN files
  - NO BITFILES OR PROJECTS
- Fri 5/7 @ 4pm: Final Project Report
  - This is worth a checkpoint grade
  - And partner evaluation
  - Turn in to TA in the lab

Checkoff Procedures (1)

- File Submissions
  - Submit your *.V and *.EDN files
  - Use the "Project Submission Directory" link that is on your U:\ drive
- Make sure you submitted files compile
  - Test this ahead of time!!
  - Bad submissions waste a LOT of time

Checkoff Procedures (2)

- Sign up for a Checkoff Slot
  - You can change up till checkoff time
  - Early slots are better
  - ALL FILES DUE BY 10AM!
- Show up at LEAST 20min early
  - If there's a problem you forfeit your slot
  - We will be behind, but don't count on it

Checkoff Procedures (3)

- We'll compile files ahead of time
  - You'll want to be there if things break
- BOTH YOU AND YOUR PARTNER MUST BE PRESENT!
  - We need to talk to you both
- We will test your project
- We will ask you some questions

Testing Requirements

- Dip-Switches
  - Local Address (3bits minimum)
  - Remote Address (3bits maximum)
- Routing Tables
  - Submit 3 versions of your router
  - With a "_1.v", "_2.v" and "_3.v"

Test Networks 1&2

- Router Configuration 1
  - Simplest Configuration
  - Used for partial credit (not much
  - Forward all packets to Green2
  - Except those destined for this board!
- Router Configuration 2
  - Even addresses go to Blue1
  - Odd addresses go to Yellow3

Test Network 3

- This will be the hardest test
  - We're not really going to explain
- Router Configuration 3
  - Address 1,7 -> White0
  - Address 4,6 -> Blue1
  - Address 2,5 -> Green2
  - Address 3 -> Yellow3

Broadcast EC

- Must hear both streams
- You can add resources to do it
  - Extra Async FIFOs for example
  - Etc…
- Mix left and right channels separately
- MUST FORWARD BROADCAST PACKETS
  - Otherwise its insanely easy

Project Report (1)

- Look at the Report Spec
- Make sure to use our title page
- You should separately fill out partner evaluations
- You will get your project report and grade at the final exam

Project Report (2)

- Typed and properly formatted
- Minimum 12pt with 1inch margins
- Max 9 pages of text, 20 pages with diagrams
- Label all figures clearly
- Use useful signal names
- Be concise

Project Report (3)

- Document Project Functionality
  - Features
  - Inputs
- Technical Descriptions
  - Don't repeat the assignment
  - Superficial information on the modules we told you how to build
- Detailed description your SDRAM/Router
  - This should be the core of your report

Project Report (4)

- SDRAM Arbiter and Router
  - Accurate and detailed
  - Lots of figures
  - These are the parts unique to each group
- Other Components
  - Give a reasonable description
  - We already know how most things work

Project Report (5)

- Purpose and Design
  - What did you do?
  - Why did you do it?
  - What did you change later?
  - How does it work?
  - What bugs did you fix?

Project Report (6)

- Block Diagrams
  - Must be clearly labeled
  - Use descriptive signal names
  - DO NOT COPY OUR DIAGRAMS
- State Diagrams
  - Use useful state names
  - Use mnemonic labeling not binary

Project Report (7)

- Submit to fileservice
  - Same place as your project (Link on U:\)
  - Electronic version MAY BE INCOMPLETE
  - We will not grade this, we just want a copy
- Hand in paper copy in the lab
  - There will be a TA there most of the day
- Reports are by Fri 5/7 by 4pm
  - DO NOT BE LATE

Project Grading

- Checkoff
  - Tests
  - Questions
  - Extra Credit
- Report
  - Clarity
  - Usefulness
- Verilog
  - Is your verilog readable?

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