EECS 150 Spring 2004

Final Exam Review
5/12/2004

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Final Exam Info

- When & Where
  - Friday, May 14th 12:30-3:30pm
  - 10 Evans
- Bring at least 2 blue books
  - You can take extras home
- Open Book/Open Notes
- It is a DESIGN final!

Schedule

- 4:00-4:40pm: Example Final 1
  - The elevator
- 4:45-5:25pm: Example Final 2
  - The VCR
- 5:30-7:00pm: Building a FIFO
  - Writing elegant verilog
  - Timing diagrams
  - FIFOs
  - SRAM

State Machine Partitioning

- Find all the state
  - What do I need to remember?
- Pick a few logical state machines
  - How many FSMs do I want?
  - What should they represent?
- Assign state to machines
  - Given a piece of state, which FSM should remember it?

Control vs Datapath (1)

- Control
  - A general FSM
  - Bubble-and-Arc
  - Good at complication operations
- Datapath
  - Counters/Registers/Adders/etc…
  - Block diagram
  - Good at sequential operations

Control vs Datapath (2)

- More Datapath
  - Use counters
  - Use one-bit (shift) registers to delay signals
  - Use registers
- Less Control
  - Complicated to design and build
  - Difficult to debug
  - The simpler the better

Building a FIFO

- Synchronous (sort of) FIFO Description
  - Read Counter
  - Write Counter
  - Full/Empty
  - SRAM
  - 2 Cycle Handshaking (Read and Write)
  - 16 bits wide, 256 lines deep