

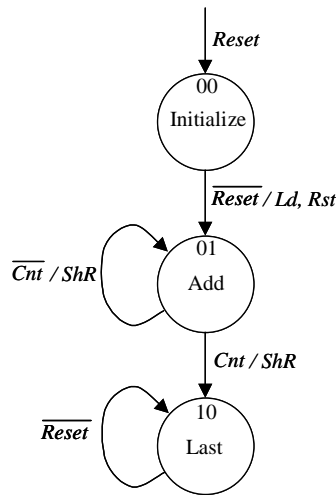
**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Science**

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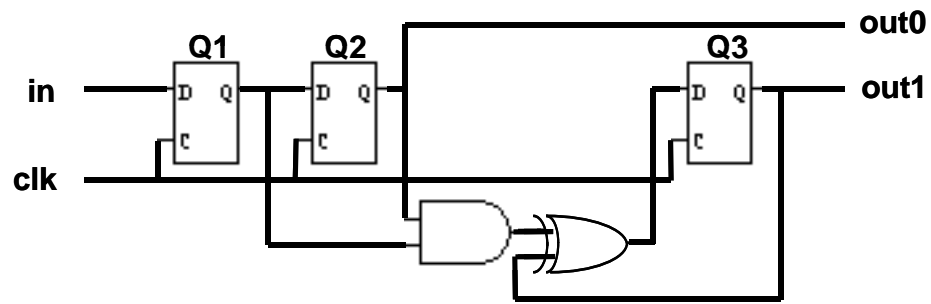
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**Problem Set # 5 (Assigned 26 February, Due 5 March)**

1. Recall Problem 2(ii) from Midterm I, which asked you to fill in a timing diagram from the controller state machine. In that problem, the state machine was a Moore machine. Consider the following variation, which specifies the controller to be a Mealy machine.



- (i) Draw out the timing chart for *Reset*, *State*, *Ld*, *Rst*, *ShR*, *Cnt*, and *Clk*, assuming *Reset* is asserted at the first rising clock edge and returns to zero before the next rising clock edge. In this case, the Mealy Machine is an *asynchronous* Mealy Machine, with the outputs direct combinational functions of the inputs and the state.
  - (ii) Repeat part (i), but this time assuming the machine is implemented as a synchronous Mealy Machine. That is, the outputs pass through positive-edge triggered flip-flops before they are visible as true outputs from the state machine.
  - (iii) Compare the timing behavior as indicated by your answers to parts (i) and (ii), as well as the Moore Machine timing behavior of the exam solutions. If there are differences in timing behavior, explain why they are different and where in the timing charts.
  - (iv) Write Verilog descriptions for the state machine reflecting the differences in implementation styles of the asynchronous and synchronous Mealy Machines of parts (i) and (ii). Briefly describe how you have structured your Verilog to distinguish between asynchronous and synchronous behaviors.
2. *State Machine Reverse Engineering*: In this problem, you will start with the circuit diagram on the following page, and derive its state transition diagram. You can do this by deriving the next state and output Boolean expressions by inspecting the circuit (recommended!), or you can attempt to enumerate all of the possible states, state transitions, and outputs.
- (i) Is this an Asynchronous Mealy, Synchronous Mealy, or Moore Machine? Briefly justify your answer!
  - (ii) Identify the inputs and outputs. Assume the flip-flops are positive-edge triggered. Derive the state diagram.
  - (iii) For your state diagram answer to part (ii), write the Verilog description for this state machine.



- (iv) Is this state machine “self-starting,” that is, since it has no explicit Reset signal, is it ever possible for the state machine start up in some state from which it cannot reach all of the other states through some sequence of inputs?
- (v) Can you describe what this circuit does?