University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150 R. H. Katz
Spring 2004

Problem Set # 2 (Assigned 29 January, Due 6 February)

1. Given the following expressions using the laws and theorems of Boolean Algebra:
   (i) W(A,B,C) = A' B' C' + A' B C' + A B' C' + A B C'
   (ii) X(A,B,C) = A' B' C' + A' B' C + A B' C + A B C
   (iii) Y(A,B,C,D) = A' B' C' D + A' B' C D' + A' B' C D + A' B C D + A B' C' D' + A B' C D
   (iv) Z(A,B,C,D) = A' B' C' D + A' B' C D + A' B C' D + A' B C D + A B' C' D' + A B' C D' + A B C' D' + A B C D'

   Use K-maps on the expressions (i)-(iv) to answer the following. Show your work in K-map form:
   (a) Find the minimized sum of products form.
   (b) Find the minimized product of sums form.
   (c) Find the minimized sum of products form of the function's complement.
   (d) Find the minimized product of sums form of the function's complement.
2. Using the same four functions as described in Problem 1, do the following:
   (a) Show how to implement each function with a Decoder and an OR gate.
   (b) Show how to implement (i) and (ii) with a 4:1 multiplexer and (iii) and (iv) with an 8:1 multiplexer.
3. Consider the following multilevel Boolean expressions:
   (i) W(A,B) = AB
   (ii) X(A,B) = A' B + A B'
   (iii) Y(X,C) = X' C + X C'
   (iv) Z(C,X,W) = X C + W

   Answer the following questions, showing your work:
   (a) What is the complexity of Y and Z in terms of gate, wire, and literal counts?
   (b) Expand Y and Z into two level networks, and repeat (a) on the result.
   (c) Find the two level canonical Sum of Products form for Y and Z.
   (d) Find the two level canonical Products of Sums form for Y and Z.
   (e) Which of your answers to (b), (c), (d) yields the "simplest" implementation of Y and Z.
4. How would you implement the functions Y(A,B,C) and Z(A,B,C) in Problem 3 using multiplexer logic? How does the complexity in terms of gates and wires compare with your answer to 3(e)?
5. Develop a minimized Boolean implementation of a multifunctional circuit that works as follows. The subsystem has four binary inputs A, B, C, D, and generates a single output bit, X. X is A if C and D are both 0, B if C and D are both 1, A + B if C is 0 and D is 1, and A B if C is 1 and D is 0.
   (a) Draw the truth table for X (A, B, C, D).
   (b) Minimize the function X using a 4-variable K-map. Write down the Boolean expressions for the minimized Sum of Products form of X.
   (c) Repeat the minimization process, this time deriving Product of Sums form.
   (d) Now implement X using an 8:1 multiplexer and no other logic other than literals. How does its complexity in terms of gates and wires compare with your answers to parts (b) and (c)?
6. Consider a combinational logic subsystem that performs a 2 x 2 multiplication function (this was presented in Lecture 2). It has two 2-bit inputs A B and C D representing binary magnitude numbers in the range 0-3, and forms the 4-bit product W X Y Z in the range 0-9. Show how to implement WXYZ using one 8:1 multiplexer for each of W, X, Y, and Z. How does the complexity in terms of gates and wires compare with the minimized answers derived in the course notes?