University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150 R. H. Katz
Spring 2004

Problem Set # 10 (Assigned 15 April, Due 23 April)
Last Problem Set!

1. Using comparators, multiplexers, and binary adder/subtractor logic blocks, design to the logic gate level a 4-bit sign and magnitude adder (i.e., a sign bit and three magnitude bits). Include an overflow indicator in your design.

2. Implement to the gate level an ALU bit slice with three operation selection inputs S_2, S_1, S_0, that implements the following eight functions of the two data inputs A and B (and carry-in C_n).

S_2	S_1	S_0	ALU operation
0	0	0	$F_i = 0$
0	0	1	$F_i = B$ minus A
0	1	0	$F_i = A$ minus B
0	1	1	$F_i = A$ plus B
1	0	0	$F_i = A$ XOR B
1	0	1	$F_i = A$ OR B
1	1	0	$F_i = A$ AND B
1	1	1	$F_i = 1$

3. Write a Verilog description for a 32-bit Booth step multiplier as presented in class. To simplify your design, you may assume an external counter that indicates to the main state machine that 32-bits have been examined. HINT: Start with the Verilog solution to Problem 3 on Midterm II, and modify it for the Booth algorithm.