University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150 R. H. Katz
Spring 2004

Problem Set # 1 (Assigned 22 January, Due 30 January)

1. Which of the following contain circuits that are likely to be combinational and which contain sequential circuits? Explain the rationale behind your answer!
   (a) A circuit that takes as input two decimal numbers A and B and outputs a 1 if A is greater than or equal to B and 0 if A is less than B.
   (b) A circuit that counts up from 0 to 9, returning to 0, and then repeating.
   (c) A circuit that implements a three position light switch: in the first position, the light is off, in the second position the light is dimly on, and in the third position, the light is on bright.
   (d) A circuit that is similar to the specification in 1(c) except that when a single switch is first pressed, the light goes from off to dimly on; when pressed a second time, the light goes from dimly on to brightly on; and when pressed a third time, the light goes off. Pressing the switch a fourth time turns it on dimly, and so on.
   (e) A circuit that multiplies two 4-bit binary numbers to form an 8-bit product.
   (f) A circuit with four binary inputs, A, B, C, D and four binary outputs, W, X, Y, Z, that works as follows. If A is 1 then W is 1, and the other outputs are 0. If A is 0 but B is 1 then X is 1. If A and B are 0 and C is 1 then Y is 1, and the other outputs are 0. If A, B, and C are 0 and D is 1 then Z is 1, and the other outputs are 0. Otherwise, all the outputs are 0.
2. Consider a digital system that works as follows. It takes as input a number in the range of 0_{10} to 15_{10} in binary and outputs a function F_3 that is 1 if the number is a multiple of 3 (i.e., 0, 3, 6, 9, 12 or 15).
   (a) Develop the truth table for this function, with four binary inputs (0000_2 to 1111_2) and the output as indicated above.
   (b) Write down the Boolean equations for the function F_3.
   (c) Characterize the complexity of this implementation by counting the number of AND, OR, and INVERTER gates of various input sizes needed to realize the output (e.g., so many 2-input ANDs, 3-input ANDs, etc.).
3. Extend the system of Problem 2 with one more output, F_6 that is 1 when the input is a multiple of 6.
   (a) Repeat parts (a) through (c) for F_6.
   (b) Describe how you can implement the function F_3 in terms of F_6 and additional logic.
4. Consider the following programmable combination lock. On the side of the lock are four dials with the numbers 0 through 9 on each one of them. From the factory, the lock comes pre-programmed with the combination 0-0-0-0. It reprogram it, first it must be opened by positioning the dials to 0-0-0-0. Then you can set a new combination on the dials. To commit to this combination, first close the lock and then

reposition the dials to 0-0-0-0. Now, to open the lock with the new combination, set the dials to the correct positions for the combination. The lock should now spring open.

(a) Define the system's inputs and outputs.

(b) Draw a finite state diagram for this subsystem, showing states, transition arcs, and logical conditions under which the machine moves from one state to the next.

5. Consider an alternative specification for a combination lock that works as follows. The lock has a single spinning dial consisting of the numbers 0 through 39. The dial can freely spin to the left or to the right. There is an indicator at the top position of the dial. The "current" number is the one directly under the indicator. To open the lock with its preset combination, you must first spin the dial to the left so that the 0 moves past the indicator. Then you spin the dial to the right to the first of three numbers of the combination, positioning the first number under the indicator. Next you spin the dial to the left but you must pass 0 underneath the indicator in doing so. Finally you spin the dial to the right, placing the final number of the combination underneath the indicator.

   (a) Define the system's inputs and outputs.

   (b) Draw a finite state diagram for this subsystem, showing states, transition arcs, and logical conditions under which the machine moves from one state to the next.