**University of California at Berkeley**
**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

**EECS 150** **Spring 2002**

# Checkpoint : MIDI Interface

This lab is an official project checkpoint. It is to be completed with a project partner on your assigned project board. Project checkpoints are designed to keep you on a weekly schedule towards completion of the project. In each week's lab, you will be asked to check-off some significant step in the design.

This lab marks a transition from what we think of as "spoon-feeding" to "hand-holding." From now in the semester, you will be given you less information on how to do the lab work. You will be making your own design decisions and figuring out your own details. You are encouraged to discuss the design problems with TAs and other students.

## 1 Objectives

The objective of this checkpoint is to demonstrate the ability to recognize MIDI commands sent from a MIDI keyboard. This demonstration consists of two milestones in the development of your project:

1. Correct electrical connection from the MIDI receptacle on the Xilinx board to the FPGA, utilizing an optoisolator.
2. Correct functioning of a MIDI parser.

The "MIDI parser" refers to a circuit that examines input bytes from a MIDI source and looks for particular patterns. This project requires a MIDI parser to recognize *note-on* and *note-off* commands. All other commands **must** be ignored (except as part of adding extra functionality to one's design). Refer to the project specification for details on MIDI commands and on MIDI hardware interfacing. Remember that there are two different ways to encode note-off commands.

## 2 Lab Assignment

First, you should read and understand the project specification. If you have any questions about the project spec, get them cleared up early.

The physical MIDI interface requires wiring-up the Motorola MOC5009 optoisolator (or the Sharp PC900V/PC900VQ) and associated discretes pack (2 resistors and 1 diode).

These components should be connected up as per Figure 6 of the project specification. Note that the 5-pin MIDI interface in the figure is drawn as if looking into the male end of a MIDI cable (not the female DIN connection on the board). The circuit will not function if the interface is wired in a mirror image.

This project checkpoint requires three circuit designs for the FPGA:

1. A UART transceiver, as designed in Lab #7.

2. A MIDI parser that takes input from the UART and recognizes MIDI note-on and note-off commands. The brains of this circuit are a simple FSM. This is a good chance to try one-hot encoding for your state machine. An output interface for the parser is suggested in the project specification and shown below (NOTE-ON and NOTE-OFF status bits which pulse when a command is received, plus KEY and VELOCITY registers to denote command contents).

3. A MIDI client that takes input from the parser and displays information about recognized commands. The NOTE-ON/NOTE-OFF, KEY and VELOCITY values produced by the parser can be displayed one at a time on the 7-segment LEDs. You may use a pair of SW5 DIP-switches to select which value to display (check the pinout sheets to see which SW5 DIP switches are still available)

Demonstrate your MIDI interface by connecting it to a MIDI keyboard in the lab and playing a few notes. Try individual notes as well as several notes at a time.

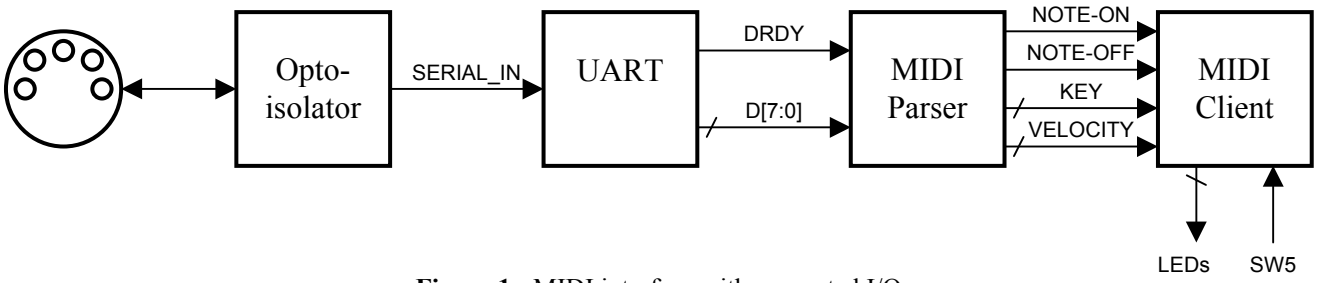


**Figure 1:** MIDI interface with suggested I/O

## 3 Acknowledgements

Original lab by J. Wawrzynek (Fall 1994).
Modifications by N. Weaver, E. Caspi, J Sampson.

Name: _____ Name: _____ Lab: _____

# 4 Check-offs
**(**MIDI Interface)

**Pre-lab**

- Wire wrap optoisolator + discretes. TA: _____ (10%)

**Lab Assignment**

- Working optoisolator + discretes (visualize output on oscilloscope) TA: _____ (20%)
- Complete MIDI interface TA: _____ (70%)

Completed on time TA: _____ (×100%)

Completed 1 week late TA: _____ (×50%)