The critical path remains in the \texttt{COMPUTE\_SUM} state. It is the path from \texttt{NEXT} through memory to \texttt{SUM}. Some of the given components have a width mismatch with respect to the original design spec from lecture, but we must use them anyway. We use a wastefully wide 16-bit adder to increment \texttt{NEXT} and a parallel pair of 8-wide multiplexors on the input to \texttt{SUM}. Note that the parallel composition of 2 multiplexors has exactly the same delay as one multiplexor. The total delay of \texttt{COMPUTE\_SUM}, hence the minimum clock cycle, is either \textbf{111\text{ns}} or \textbf{141\text{ns}}, depending on your version of the quiz. Two versions were distributed, each with different timing for components.

\begin{center}
\begin{tabular}{|l|l|}
\hline
Component & Delay \\
\hline
8-bit Register & Clk-to-Q=1\text{ns} Setup=1\text{ns} \\
8-bit wide 2-1 Mux & 3\text{ns} \\
16-bit Adder & 30\text{ns} \\
Memory & 40\text{ns} \\
Zero Compare & 5\text{ns} \\
\hline
\end{tabular}
\end{center}

\begin{center}
\begin{tabular}{|l|l|}
\hline
Component & Delay \\
\hline
8-bit Register & Clk-to-Q=1\text{ns} Setup=1\text{ns} \\
8-bit wide 2-1 Mux & 3\text{ns} \\
16-bit Adder & 40\text{ns} \\
Memory & 50\text{ns} \\
Zero Compare & 5\text{ns} \\
\hline
\end{tabular}
\end{center}

Timing diagram for \texttt{COMPUTE\_SUM} state