Building a JK-type positive edge triggered FF from a D latch (transparent on $\text{clk}$ high) can be done in two steps:

1. **Build a positive edge-triggered D-type FF from two D latches.**
   We use a simple “master-slave” configuration. To determine which latch needs an inverted clock, consider what the latches do to make the FF trigger on a positive clock edge. During a positive clock edge, the first latch must capture a new value (transition to hold), while the second latch must pass that new value through (transition to transparent). Thus it is the second latch that is transparent on $\text{clk}$ high. The first latch needs an inverted clock.

2. **Build logic for JK-type inputs.**
   Conceptually, we need to implement a 4-to-1 multiplexor for the D input. Controlled by J and K, the mux selects from 4 possible next values: hold, jam, kill, or toggle. Implementing the mux using an AND-OR network, it is actually possible to omit the AND gate for the 0-valued “kill” case (J=0, K=1).