Professor Fearing EECS150/Problem Set 4 Fall 1998

**Due at 5 pm, Thu. Sep. 24 in box outside 218 Cory Hall**

Quiz 1. 2-330 pm Tues. Sep. 29, 10 Evans

Reading Katz: 6.1:6.3,8.5, 10.4

1. FSM/Counter combination (25 pts)

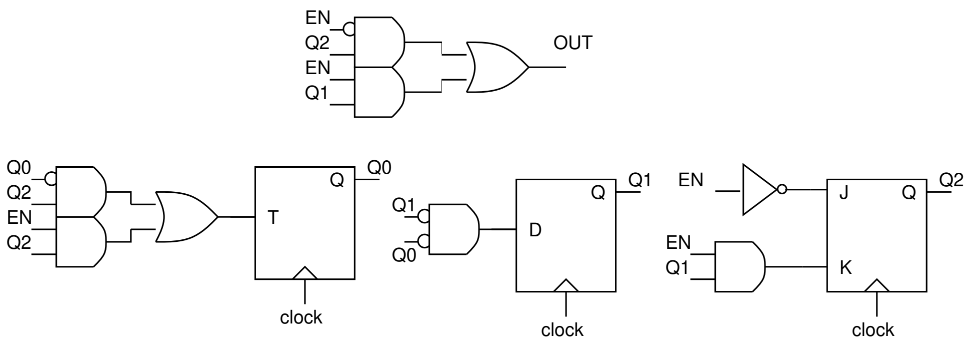
Design a system, using two CB2CLED bidirectional counters, which counts in the sequence 5, 6, 7, 8, 9, 15, 14, 13, 12, 5, 6, 7, ... Hint: use four M2_1 to select the count value to load. Consider the two counters as your data path, and design a simple finite state machine controller which will control loading and the up/down direction appropriately.

2. FSM Design (25 pts)

Design a Moore type FSM for a sequence recognizer. The FSM should assert OUTPUT for one clock cycle for every (possibly overlapping) sequence "111" detected in the synchronized input data stream Z. Show timing diagram, state diagram, state table, and schematic using synchronous reset T-type FFs from the Xilinx library (FTRSE).

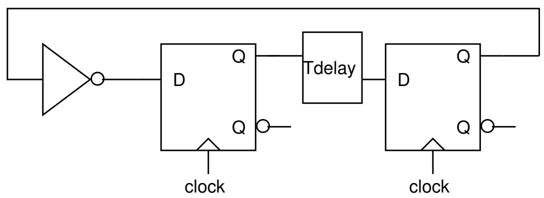
3. FSM Analysis (20 pts)

Make a state transition table and state diagram for the following circuit (with input EN.H and output OUT.H):




4. Timing Analysis (25 pts)

Using a timing diagram, determine the minimum clock period for this circuit. (Parameters: $T_{setup} = 5$ ns min, $T_{hold} = 3$ ns, $2.5 < T_{CKO} < 12$ ns, $T_{delay} = 10$ ns and inverter propagation $6 < t_p < 9$ ns.) Also, determine the fastest inverter which could be used in this circuit (i.e. if the inverter were faster than 6 ns, is there any potential problem?)




5. (5 pts)

How many possible different boolean functions are there of 5 variables? How big a memory (look up table) would be needed to store any one function of 5 variables?