Professor Fearing EECS150/Problem Set 10 Fall 1997

Due at 5 pm, Thu. Nov. 13 in box outside 218 Cory Hall

1. Microcode for FSM emulation (30 pts)

In this problem you will emulate a two bit up/down synchronous counter using the micro-programmed control unit shown below. The counter you are emulating has two inputs: CEN.H (count enable) and UP.H, and two outputs Q0.H and Q1.H. If UP and CEN are asserted the outputs Q0 and Q1 should increment. If CEN is asserted and UP is not asserted the counter should count down. Let $CEN \cdot UP$, and $\overline{CEN}$ be connected to D0, and D1 respectively on the 4:1 mux. Write a micro-program which will emulate the up/down counter listing your program in mnemonic and numeric form. (Note that branches only occur when test variables are asserted; do not add any inverters. Also note that your state machine may not necessarily change states on the same clock edge as the MCU clock.) Show a timing diagram with the output register Q0, Q1, CLOCK, UP, and CEN. (Choose inputs to visit states in the sequence S0-S1-S2-S1-S0). On your diagram, label each clock period with the current address (micro-program counter contents).

2. Micro program control unit expansion (30 pts)

Now design another version of the MCU, which has 15 output bits, 1024 microinstruction addresses, and 16 branch conditions, using a single 8K by 8 bit ROM. Show a detailed block diagram of the controller. (Hint: consider extra registers and extra clock phases [synchronously generated of course!]).

3. Microcode for CPU control (35 pts)

Using the micro-programmed control unit below as a starting point, draw a detailed block diagram of an MCU (making sure to specify widths of ROM and registers) which could control the processor of Figure Ex11.13 in the text, using a vertical micro-code format. Specify which controller outputs need to be latched (if any). List, in symbolic form, the micro-code needed to implement the ADD Ra, (Rb)offset instruction.