# EECS150 Fall 2013 Checkpoint 3: Image Processing Pipeline Proposal

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Due week of Nov. 14.
Revision 1.2, Nov. 13.

**References**

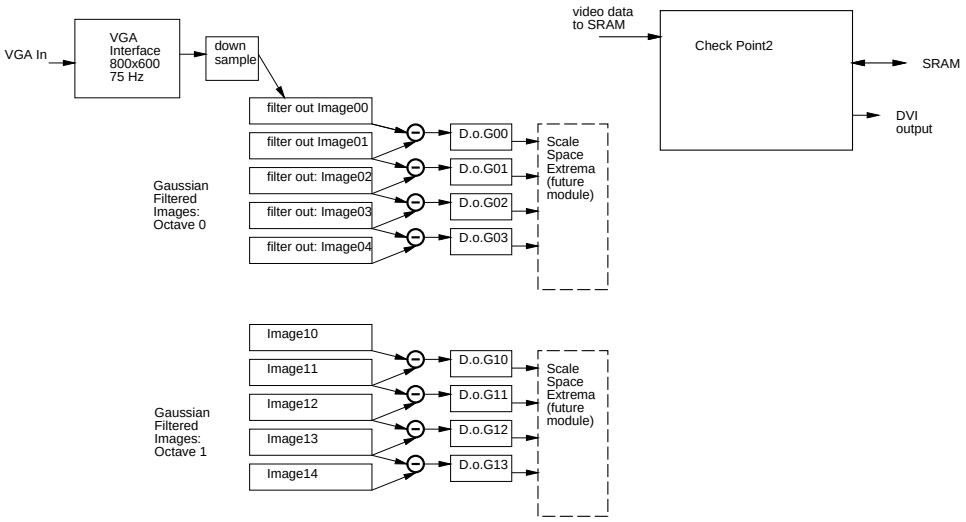
1. Bonato, V.; Marques, E.; Constantinides, G.A., "A Parallel Hardware Architecture for Scale and Rotation Invariant Feature Detection," *Circuits and Systems for Video Technology, IEEE Transactions on,* vol.18, no.12, pp.1703,1712, Dec. 2008
2. CS150 Lectures #14, #15

For this checkpoint, you will be producing a technical proposal for the design of the Difference of Gaussian (DoG) portion of your class project. Through this process you will practice converting an algorithmic description to a hardware design. Ultimately, this proposal will serve as the plan for completing the DoG portion of the SIFT algorithm in your project design.

Referring to the block diagram below, you will plan the design of the Gaussian filtering block, and difference of Gaussian calculations. The DVI frame buffer will be used to display one of: 1) VGA input 2) output of the Gaussian filter blocks or 3) output of DoG calculations. The output should be selectable without recompiling. If time allows, the scale-space extrema and blocks and MicroBlaze interface can be added, but are not required for this checkpoint.

**Design Specification**

1. Choose $s = 3$ for image frames for SIFT. Thus there will be 6 images in the pipeline including the original image.
2. Use a 5x5 separable window FIR filter for the Gaussian blurring.
3. The VGA image (800x600) at 75 Hz is probably too fast for the FIR pipeline. In your design, you can try 400x300 or 200x150. You will need to downsample the VGA image, and upsample back to 800x600 for displaying on DVI.
4. Use at least 2 octaves of Gaussian filtering, with the second octave having half the horizontal and vertical resolution of the first octave.




**Design Review**

The deliverable for this checkpoint is just the document describing your design plan. You will turn in this document by checking it in to your team repository. (We suggest adding it with all supporting files in a "proposal" directory at the repository root.) This document should include:

1. Detailed block diagram of the data path for the Image Processing Pipeline, including Gaussian filter banks, Difference of Gaussian banks, down sampling, upsampling, interface connections to VGA data stream, and connections to frame buffer from Checkpoint 2. Level of detail should be registers, muxes, arithmetic elements, etc. Specify widths of all data paths. (Estimate necessary resolution needed for fixed point arithmetic.)

2. Identify in a seperate list all the input control signals and output status signals from the datapath.

3. Describe detailed operation sequence for the image processing pipeline in RT Language.

4. Draw a state diagram for the controller for the image processing pipeline, including any needed interface with VGA or frame buffer. As appropriate, detail interface to other major blocks with state or timing diagrams.

5. Outline testbench specifications describing the cases you want to test, expected output for a succesful design and likely failure modes.

You will meet with your GSI to get feedback on your group's design. **Please bring a printout of your design documents to the meeting.**