Professor Fearing EECS150/Problem Set 9 Fall 2013

Due at 12 pm, Thu. Nov. 21 (homework box under stairs)

(This problem set may be done in a group of maximum 2 students, with 1 unique writeup to be turned in per group.)

Reading DDCA p. 239-243, 250-252.

1. (45 pts) Adders.

For each part, use 4 bit blocks, 2 input gates only. Estimate number of 2 input gates used (assume AND, NAND, OR, NOR, and that inverters can be considered part of 2 input gates). Also estimate worst case delay.

a. A 16 bit ripple carry adder.

b. A 16 bit carry look ahead adder.

c. A 16 bit carry select adder.

2. (35 pts) Multiplier

Design an unsigned combinational multiplier (no flip-flops or controller) for multiplying the unsigned constant value $297_{TEN} = 0xc7$ by the 4 bit variable $Z[3:0]$. Using only full-adder cells and inverters, draw a circuit that implements the multiplier using carry-save addition. Estimate delay from input to output. How many full-adder cells are needed?

3. (20 pts) Logic assertion levels.

Signals A.L, B.L, and C.L are asserted low (i.e. $l = 1, h = 0$). For example if A.L is high, it is a logic "0". Signals X.H, Y.H, and Z.H are asserted high (i.e. $l = 0, h = 1$). For example if X.H is high, it is a logic "1". You are given a two input circuit with inputs m, n and output $f(m, n)$ which has the following input-output function:

m	n	f
l	l	h
l	h	l
h	l	l
h	h	l

Determine the Boolean functions for the following:

a. $Z.H = f(X.H, Y.H)$

b. $C.L = f(X.H, Y.H)$,

c. $C.L = f(A.L, B.L)$, and

d. $Z.H = f(X.H, A.L)$.

(Note that signals are on wires, and no physical inverters are added to any wires.)