Professor Fearing EECS150/Problem Set 8 Fall 2013

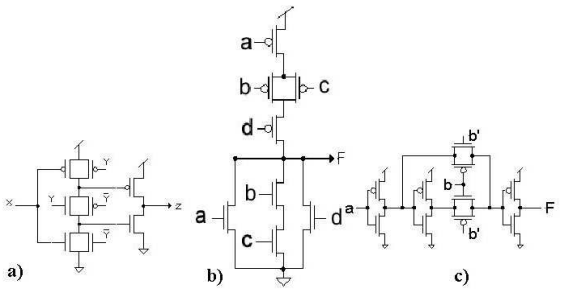
Due at 12 pm, Thu. Nov. 7 (homework box under stairs)

(This problem set may be done in a group of maximum 2 students, with 1 unique writeup to be turned in per group.)

1. (25 pts) CMOS.

a,b,c. Draw its common symbol or state the equivalent Boolean expression for the circuits to the right.

d. Implement the function $y = \overline{(a+b)(c+d)}$ using CMOS transistors with the minimum number of transistors.

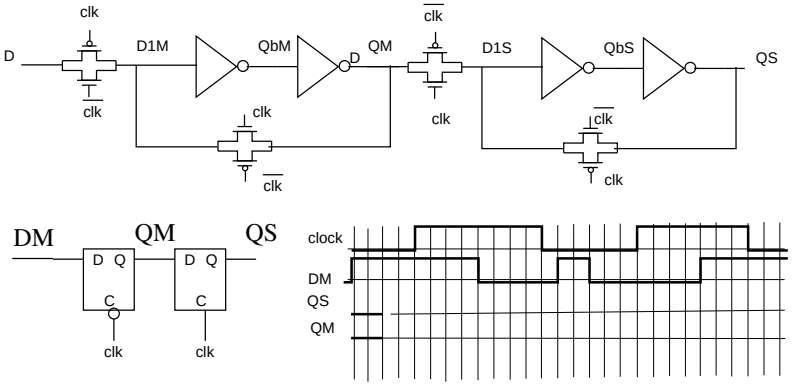


2. D- master-slave FF Timing (40 pts)

a. Draw a timing diagram for the D master-slave FF circuit below, assuming unit delay through the inverters and transmission gates, and showing signals $clk, DM, D1M, QbM, QM, D1S, QbS, QS$.

b. Modify the D-master-slave FF circuit below, using minimum number of gates, to add a synchronous reset.

c. Modify the D-master-slave FF circuit below, using minimum number of gates, to add a clock enable.



3. Clock Skew (35 pts)

For this problem consider the parameters $T_{setup} = 1.1$ ns min, $T_{hold} = 0$ ns, $T_{CKO} < 1.3$ ns, $T_{delay} = 20$ ns and inverter plus interconnect propagation 4 ns. For each question below, justify your answer with a timing diagram.

a. With delay $T_0 = T_1 = 0$ ns, what is the maximum clock speed?

b. What is the maximum $T_1 - T_0$ for proper operation?

c. What is the minimum $T_1 - T_0$ for proper operation?

d. In Xilinx Virtex5 FPGA designs, how can you prevent indeterminate delays on the clock line due to random routing?