Professor Fearing EECS150/Problem Set 7 Fall 2013

**Due at 12 pm, Thu. Oct. 24 (homework box under stairs)**

(This problem set may be done in a group of maximum 2 students, with 1 unique writeup to be turned in per group.) Reading: DDCA 3.4.

1. Video Encoder (35 pts)

Consider the video encoder from Checkpoint 1.

a. Describe in words the operation of the CountRegion.v module.

b. Describe in words the operation of the CountCompare.v module.

c. Draw a detailed block diagram for the PixelCounter.v module, showing inputs, outputs, registers, counters, CountCompare, and CountRegion blocks.

d. Draw a sketch of a rectangular screen which shows the relation of XActive and YActive regions to the whole frame, including blanking regions.

2. Finite State Machines, Moore vs. Mealy (35 pts)

Consider a sequence detector which detects the possibly overlapping pattern "101" in a synchronized input sequence IN. A global reset brings the sequence detector to the initial state corresponding to a "0" input.

a. Draw a state diagram for a Mealy type FSM which outputs DETECT for one clock cycle every time "101" is detected on IN.

b. Repeat part a. using a Moore type FSM.

Consider two possible synchronized input streams A and B. A mux with 1 bit select line SEL is used to select source A (SEL=0) or source B (SEL=1) for the sequence detector.

c. Draw a state diagram for a 2 state Mealy-type FSM whose output SEL alternates between SEL=0 and SEL=1 as soon as input DETECT is asserted and maintains the current output SEL until the next assertion of input DETECT.

d. Repeat part c. but for a Moore type FSM.

Consider serial streams A=0101011101 and B=0000010100.

e. Consider the Mealy FSM sequence detector of part a. with an input mux controlled by the Mealy FSM of part c. Draw a timing diagram showing clock, A, B, DETECT, SEL.

f. Consider the Moore FSM sequence detector of part b. with an input mux controlled by the Mealy FSM of part c. Draw a timing diagram showing clock, A, B, DETECT, SEL.

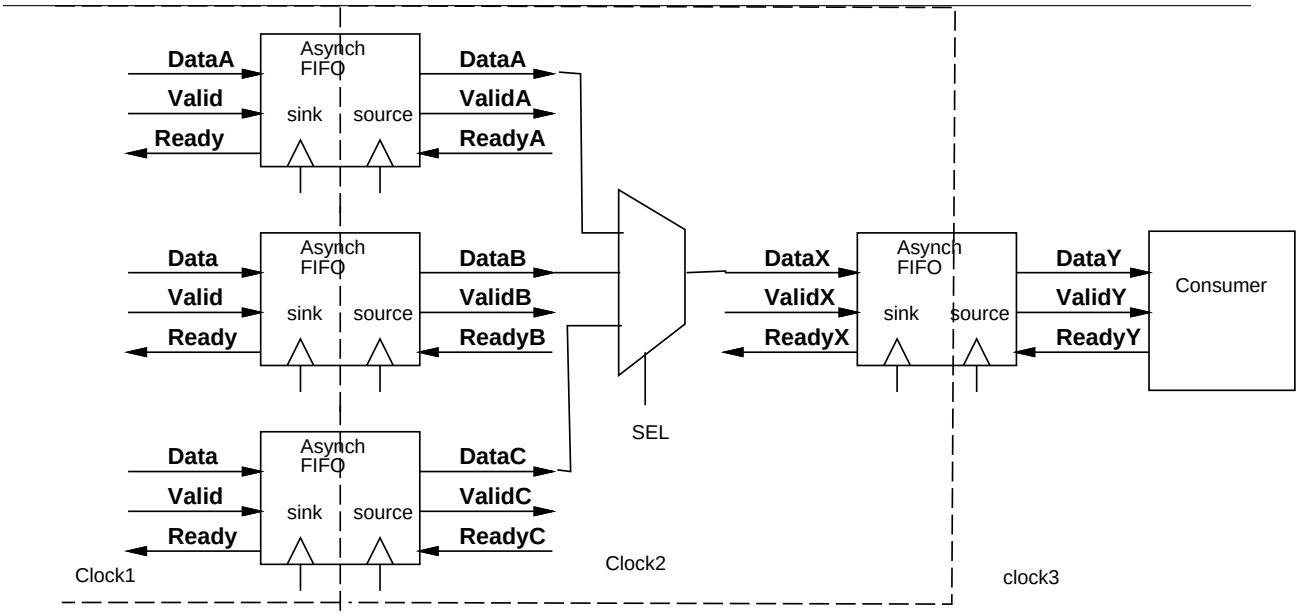
g. For part e. and f., explain any operational differences or problems found.

3. Round-Robin Arbiter and FIFOs (30 pts)

Consider the data path below.

a. Draw a state diagram for a round robin arbiter which, when ReadyX is asserted, will read data from FIFOs in order A,B,C,A,... if a FIFO has data ready. If a read FIFO is not asserting Valid, the scheduler should skip ahead to the next source in order. The FSM should be in clock domain 2 and generate all needed control signals, i.e. explain how to calculate the control signals from present state and inputs.

b. Consider that at reset FIFO A,B,C contain respectively 3,2, and 1 data words. Clock2 runs at 10 MHz, and clock3 runs at 45 MHz, and Consumer can process one word every clock cycle. Draw a timing diagram showing clock2, Data, Ready, and Valid for A,B,C,X,Y. For timing diagram, data should be labelled A0, A1, etc. Assume the FIFO is setup in Read w/FWFT mode.


DataA
Valid
Ready
Asynch FIFO
sink
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DataA
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sink
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DataB
ValidB
ReadyB
Data
Valid
Ready
Asynch FIFO
sink
source
DataC
ValidC
ReadyC
SEL
DataX
ValidX
ReadyX
Asynch FIFO
sink
source
DataY
ValidY
ReadyY
Consumer
Clock1
Clock2
clock3