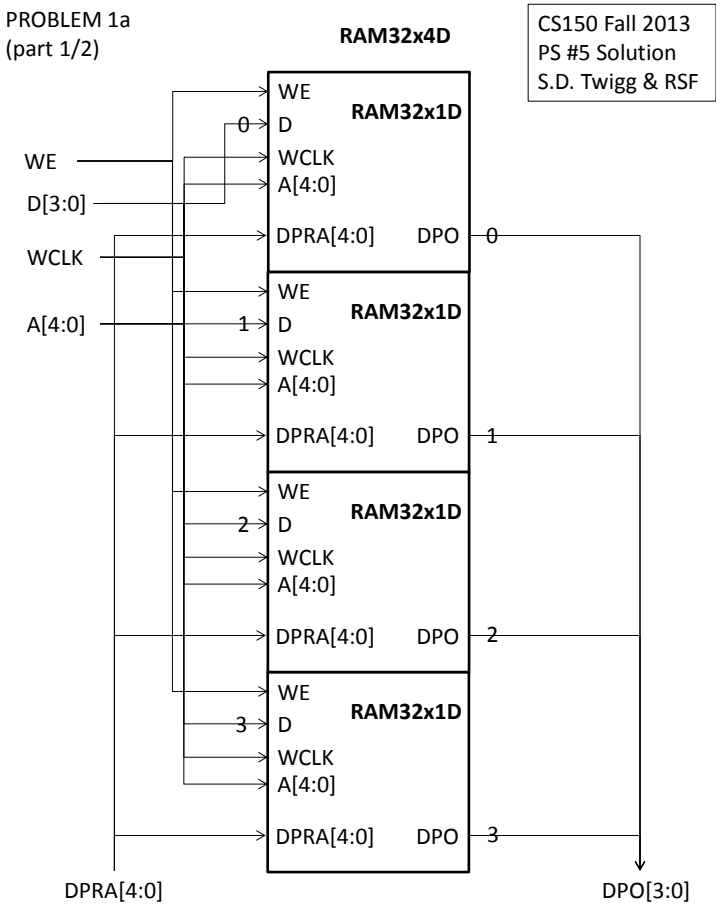
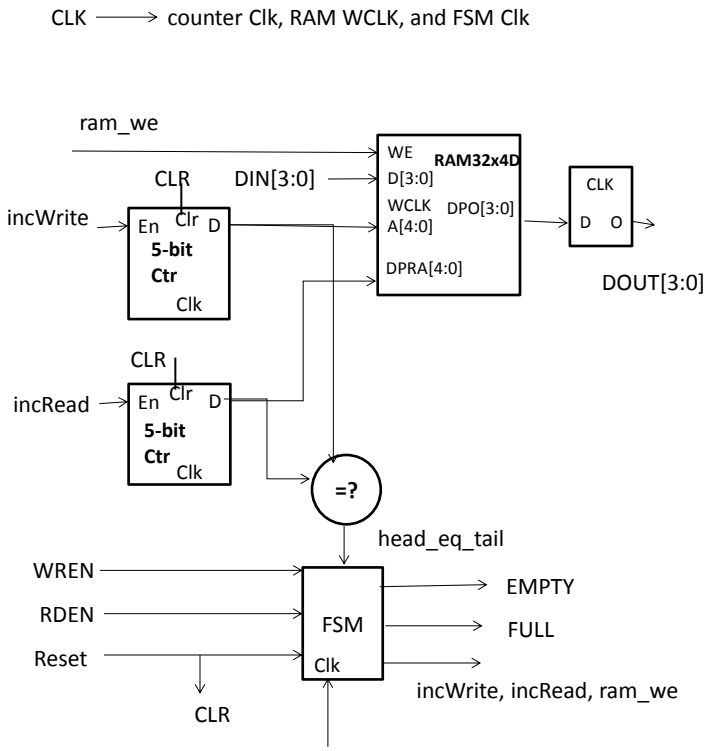
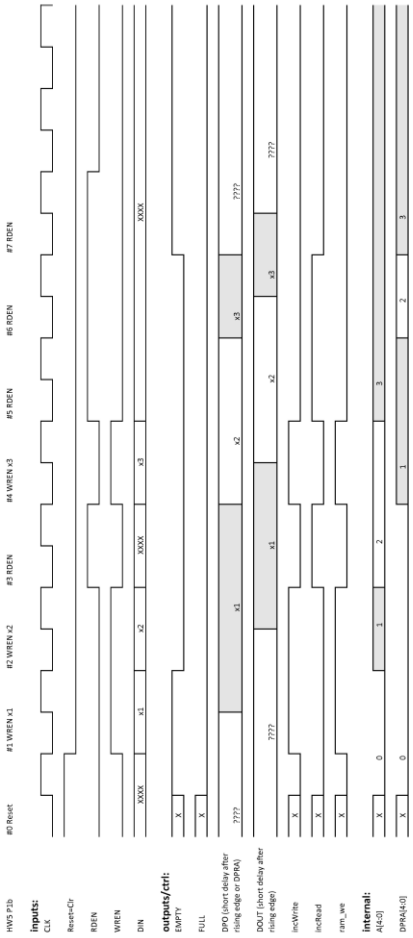
PROBLEM 1a
(part 1/2)

CS150 Fall 2013
PS #5 Solution
S.D. Twigg & RSF



PROBLEM 1a
(part 2/2)

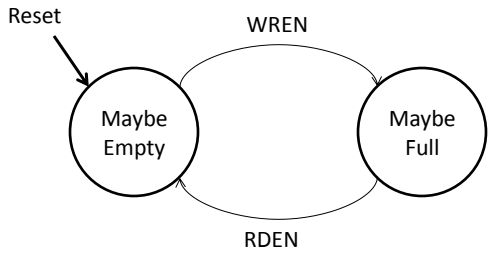




PROBLEM 1b

Note: Delay is exaggerated to 0.5 clock cycle from rising edge of clock for all signals except DPO and DOUT

PROBLEM 1c

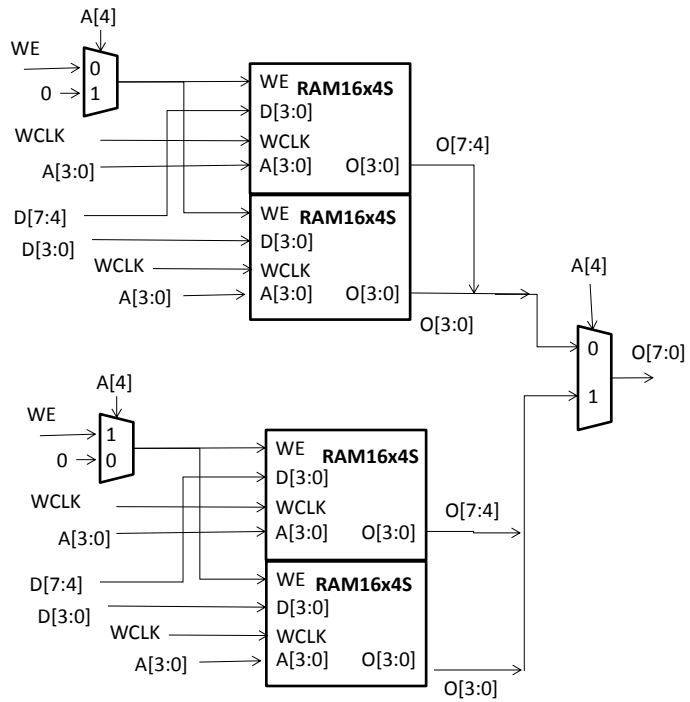


FULL = (Maybe Full) && head_eq_tail
EMPTY = (Maybe Empty) && head_eq_tail

incRead = !EMPTY && RDEN
incWrite, ram_we = !FULL && WREN

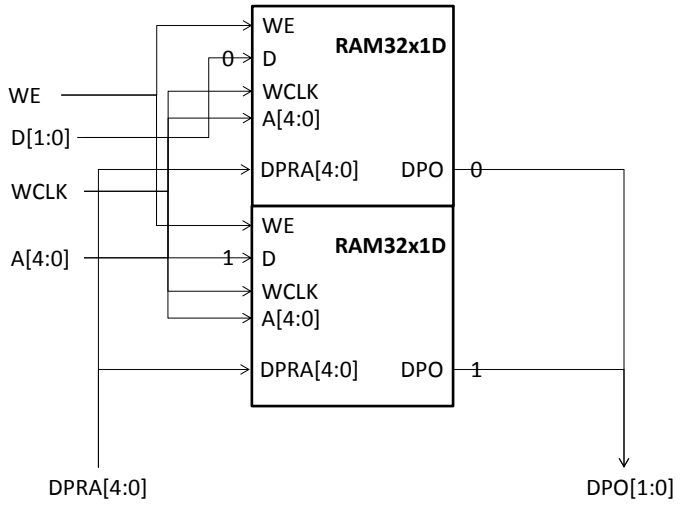
PROBLEM 2a

RAM32x8S



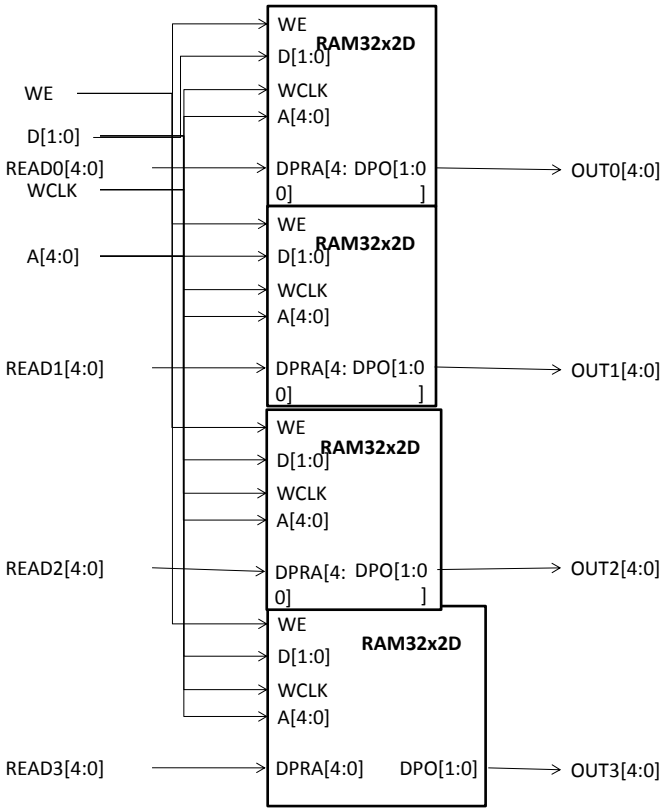
PROBLEM 2b
(part 1/2)

RAM32x2D



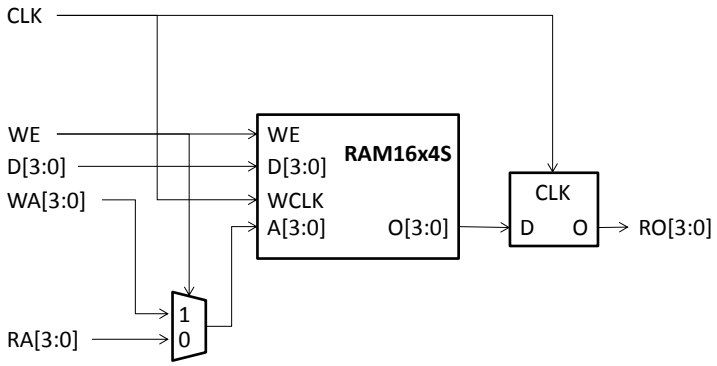
PROBLEM 2b
(part 2/2)

RAM32x2D w 4 asynch read ports



PROBLEM 2c

RAM16x4S w 4 sync read, sync write



Problem 3.
Note: MTBF = Tc/(N*To)*exp((Tc-tsetup)/tau)
Where N is the number of changes per second (100 million).
MTBF= 100 years = 3.15 billion seconds
To = 20 ps
Tsetup = 50 ps
Tau = 30 ps
Tc is clock period to find = 1950 ps = 1.95 ns