Professor Fearing EECS150/Problem Set 5 Fall 2013

Due at 10 am, Thu. Oct. 10 (homework box under stairs) Reading DCA p. 151-154, Xilinx Library p. 108-111, 256-258, 269-271; Virtex5 Users Guide p. 178-188, skim XST 129-151.

1. FIFO Design (50 pts)

This problem considers the design of a 32 entry FIFO (first in first out) register file using four **dual port** RAM32X1D (p.269 of *Libraries Guide for HDL Design*). The FIFO has 4 bits in $DIN[3:0]$ and 4 bits out $DOUT[3:0]$, synchronous inputs WREN, RDEN, Reset, and CLK, and 2 outputs $Full$ and $Empty$. The data path consists of four RAM32X1D 32×1 RAM, an output register with clock enable, a detector for Full/Empty, and two synchronous 5 bit up counters with reset and count enable. Assume that inputs WREN, RDEN, and DIN are synchronized with CLK. If FIFO is $Full$, ignore WREN, and in case the FIFO is $Empty$, ignore RDEN. (Assume FSMs communicating with the FIFO will handle the Full/Empty signals, and prevent read or write errors.)

a. Draw a detailed block diagram for the data path, carefully showing inputs and outputs.

b. Draw a functional timing diagram showing example operation of the FIFO, including $Full$ and $Empty$, and all control and data signals. Use as example operation Reset, WREN DIN=x1, WREN DIN=x2, RDEN, WREN DIN=x3, RDEN, RDEN, RDEN. Where x1, x2, x3 represent data values.

c. Draw a state diagram for the controller FSM for the FIFO, being sure to label the active outputs associated with each state.

2. RAM blocks (35 pts)

(For this problem, draw detailed block diagrams, don't write Verilog.)

a. Using as many of the RAM16X4S 16 deep by 4 wide static synchronous RAM as needed, combined with multiplexers and simple logic, design a 32×8 RAM with synchronous write.

b. Using as many of the RAM32X1D 32 deep by 1 dual static synchronous RAM as needed, combined with multiplexers and simple logic, design a 32×2 RAM with a synchronous write port, and 3 additional asynchronous read ports.

c. Using as many of the RAM16X4S 16 deep by 4 wide static synchronous RAM as needed, combined with multiplexers, registers and simple logic, design a 16×4 RAM with one synchronous (registered) read port and one synchronized write port. This dual port RAM emulation will need two clock cycles to perform a write and read as there is only one address bus. Thus design a simple FSM which can control the memory operations.

3. Metastability and Synchronization (15 pts)

A synchronizer is built from a pair of flip-flops with $t_{setup} = 50$ ps, $T_o = 20$ ps, and $\tau = 30$ ps. It samples and asynchronous input that changes 10^8 times per second. What is the minimum clock period of the synchronizer to achieve a mean time between failures (MTBF) of 100 years?