

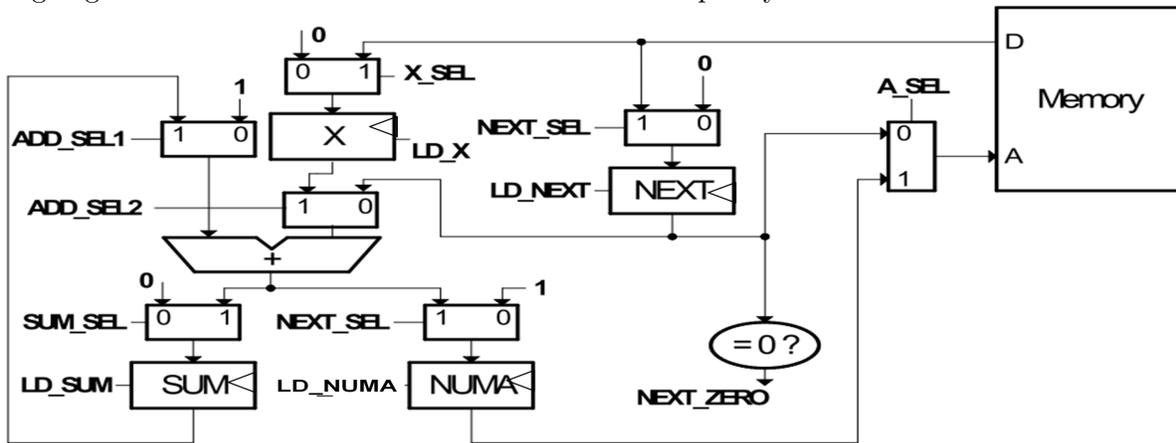
1. (25 pts) List Processor Timing

The list processor as discussed in lecture is described in RT Language as:

1. $X \leftarrow \text{Memory}[\text{NUMA}], \text{NUMA} \leftarrow \text{NEXT} + 1;$
2. $\text{NEXT} \leftarrow \text{Memory}[\text{NEXT}], \text{SUM} \leftarrow \text{SUM} + X;$

Due to routing in Xilinx, wider data paths can have greater delays. Assume delays: clk-to-Q 1 ns, setup time 1 ns, 8 bit Mux 3 ns, 16 bit Mux 4 ns, 8 bit adder 8 ns, 16 bit adder 10 ns, NextZero 2 ns, memory 20 ns. Consider the data path below.

- a. Draw a timing diagram showing the critical path for both states.
- b. Assume the finite state machine controller requires NextZero to be settled 12 ns before the rising edge of the clock. What is the maximum clock frequency?



2. (25 pts) Infinite impulse response filtering

Consider a digital signal processor with input $x[n]$ and output $y[n]$. For an all-pole IIR filter, the general form is

$$y[n] = \sum_{k=1}^N a_k y[n - k] + b x[n].$$

For this problem, let $N = 3$, then the IIR filter is given by

$$y[n] = a_1 y[n - 1] + a_2 y[n - 2] + a_3 y[n - 3] + b x[n].$$

In RT Language, the IIR filter can be described as:

$$Y1 \leftarrow b * x[n] + a_3 * Y3 + a_2 * Y2 + a_1 * Y1, Y3 \leftarrow Y2, Y2 \leftarrow Y1;$$

- a. Draw a block diagram for the IIR data path described by the RT Language.
- b. Given delays $T_{mult}, T_{add}, T_{D-to-Q}, T_{setup}$ find the critical path and estimate the maximum operation frequency.
- c. Can pipelining improve the clock rate of the IIR filter? If yes, show by modifying the block diagram from part a., otherwise explain why not.

3. (30 pts) Finite impulse response filtering

Consider a digital signal processor with input $x[n]$ and output $y[n]$. For an all-zero FIR filter, the general form is

$$y[n] = \sum_{k=0}^{N-1} b_k x[n - k].$$

For this problem, let $N = 4$, then the FIR filter is given by

$$y[n] = b_0 x[n] + b_1 x[n - 1] + b_2 x[n - 2] + b_3 x[n - 3].$$

In RT Language, the FIR filter can be described as:

$Y \leftarrow b_0 * x[n] + b_3 * X3 + b_2 * X2 + b_1 * X1, X3 \leftarrow X2, X2 \leftarrow X1, X1 \leftarrow x[n];$

- Draw a block diagram for the FIR data path described by the RT Language.
- Given delays $T_{mult}, T_{add}, T_{D-to-Q}, T_{setup}$ find the critical path and estimate the maximum operation frequency.
- Show how pipelining can improve the clock rate of the FIR filter, by modifying the block diagram from part a.
- Write RT Language for the FIR filter with pipelining.

4. (20 pts) Serial Multiplier

A serial multiplier is shown below. The A and B registers are 4 bits, with initial values 4'b1110 and 4'b1001 respectively. Complete the table for all operation steps.

step	B	A	HI	LOW	sum	carry
0	1001	1110	0	0	0	0
1						
...						

