1. (20 pts) Datapath and control I
For the datapath below, determine a sequence of operations which will exchange the contents of Acc and Sum. (Contents of register A can be discarded). The data path is 8 bits wide. Φ is the clock.
   a. Describe the necessary operations using a Register Transfer Level description. How many clock cycles are required?
   b. Draw a functional timing diagram for the circuit including Φ, LoadA, LoadSum, EnAdd, LoadAcc, ClearA, ClearSum which shows the RTL operation of part a.
   c. Draw a state diagram for a controller which starting in Idle, when given a Start signal, will swap Acc and Sum and then go back to the Idle state.

2. (30 pts) Datapath and control II
For the datapath below, determine a sequence of operations which will perform the operation \( z = 4 \times x + 2 \times y \), where initial values are Acc = x, Sum = y and answer z is stored in Sum.
   a. Describe the necessary operations using a Register Transfer Level description. What is the minimum number of clock cycles required?
   b. Draw a functional timing diagram for the circuit including Φ, LoadA, LoadSum, EnAdd, LoadAcc, ClearA, ClearSum which shows the RTL operation of part a.
   c. Draw a state diagram for a controller which given a Start signal, will perform the operation, and then go back to the Idle state.
   d. Implement the control FSM and data path as separate Verilog modules.

3. FSM Design (25 pts)
Design a Moore type FSM for a sequence recognizer. The FSM should assert Output for every sequence “110” detected in the synchronized serial input stream Z.
   a. Show state diagram for sequence recognizer.
   b. Show timing diagram (Clock, Z, Q[2:0]) for the input sequence “01011011101”, with left most bit arriving first.
   c. Implement the FSM in Verilog.

4. Verilog Testbench (25 pts)
Write a Verilog test bench for the FSM in question 3, making sure that all state transitions are covered.