Professor Fearing Problem Set 10 Fall 2013

(This problem set will not be collected or graded, but the solution will be available Thurs. Dec. 12.)

1. Fast up counter.

An up counter has next state decoder `NS = PS + 1` . Design a 16 bit``Carry Look Ahead'' incrementer (add 1) using 4 bit blocks, 2 input gates only. Estimate number of 2 input gates used (assume AND, NAND, OR, NOR, and that inverters can be considered part of 2 input gates). Also estimate worst case delay. Compare to delay and gate count for ripple carry adder and CLA from PS9.1.

2. Clock generation

A digital designer group wants to run a FIR filter block at 1/16 the clock speed of the main system clock. The FIR filter block is proposed to connect directly to other blocks in the system without using an asynchronous FIFO. The main system clock, and divided clock are distributed using built in Xilinx global clock buffers.

a) Consider clock generation using divide by 16 with a ripple carry counter (Lec 25, slide 28) . Explain with the aid of a timing diagram, issues which might arise either on input or output of FIR module (either data or control conections).
b) Consider clock generation using divide by 16 with a synchronous counter. Explain with the aid of a timing diagram, issues which might arise either on input or output of FIR module.
c) Consider clock generation using the builtin Xilinx DCM_ADV clock manager (Chap. 2 of Virtex-5 FPGA User Guide). How does using this primitive avoid problems seen in a) or b)?

3. Soft Errors

(Referring to lec26, slide 6, and Xilinx ug116.pdf.) Assume a Virtex-5 design uses 1 Mb for configuration memory and 1 Mb of block RAM. Assume cross-section is in sq.cm.

a) Assuming 15 neutrons/sq.cm//hr (sea level). How many hours could you expect before the first soft failure is seen in config and block RAM?
b) How can you detect or recover from soft errors in Xilinx Virtex5 FPGA?
c) At 12 km, neutron flux could be 10,000 times larger than at sea level. With a fleet of 1000 aircraft at 12 km equipped with Virtex-5 avionics, how many hours would you expect between soft failures anywhere in the fleet?

4. Error Correction

Design a single bit error correction, double bit error detection Hamming code for 8 bit data.
State the positions of the parity bits, and which bits of the codeword each parity bit protects.

5. Power/Energy

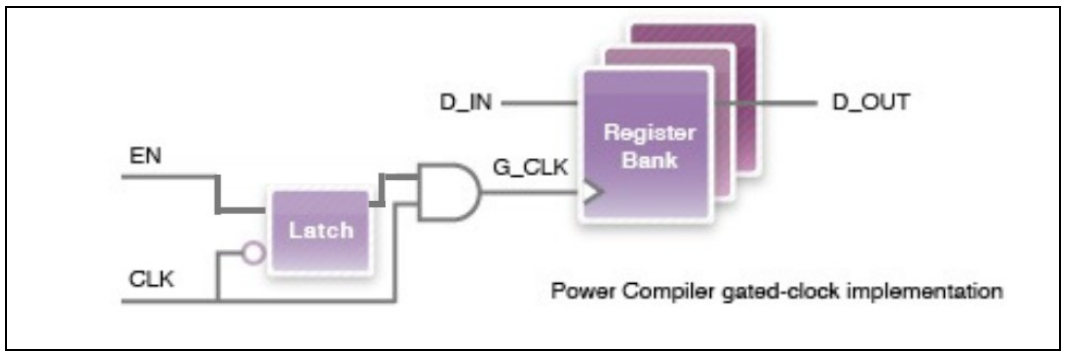
Designer A decides to duplicate her datapath in an accelerator such that the compute throughput can be increased by 2X (you can assume the application contains enough parallelism for this to happen) when she runs the accelerator at the same clock frequency.

a) Designer B tries to match this performance gain by increasing the voltage of his circuit (assume the max frequency a CMOS circuit is positively related to the voltage at which it runs). In terms of dynamic power consumption, do you think his solution is better or worse than that of Designer A ? Why?
b) With the duplicated datapath, Designer A can afford to reduce the clock frequency by half yet still achieve the throughput of the original accelerator. If she does not lower the voltage of the circuit, how does this reduction of clock frequency effect the overall power of the circuit? How

does it effect the overall energy consumption for running the application? Explain your reasoning. (Note: the baseline used in this question is the accelerator with a duplicated datapath.

6. Power Down circuit

Gating the clock is generally a very bad idea. However disabling the clock can drastically reduce power consumption for a block of circuitry. The circuit below claims to be a safe way to generate G_CLK. Show with a timing diagram whether this is true or not.



7. Architecture for Power reduction.

A. Chandrakasan (CS150 F'89) and R. Brodersen [IEEE 1995] proposed three architectures for a sum/comparator. Assuming delay Tdq, Tsum, Tcomp and Tsu, determine throughput and minimum clock period for each design.