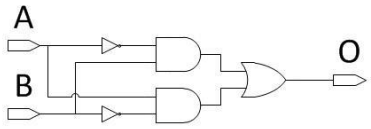
(Vers 1.1)

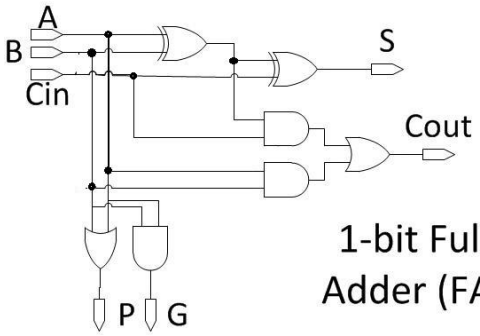
Problem 1: Adders.

For each part, use 4 bit blocks, 2 input gates only. Estimate number of 2 input gates used (assume AND, NAND, OR, NOR, and that inverters can be considered part of 2 input gates). Also estimate worst case delay.

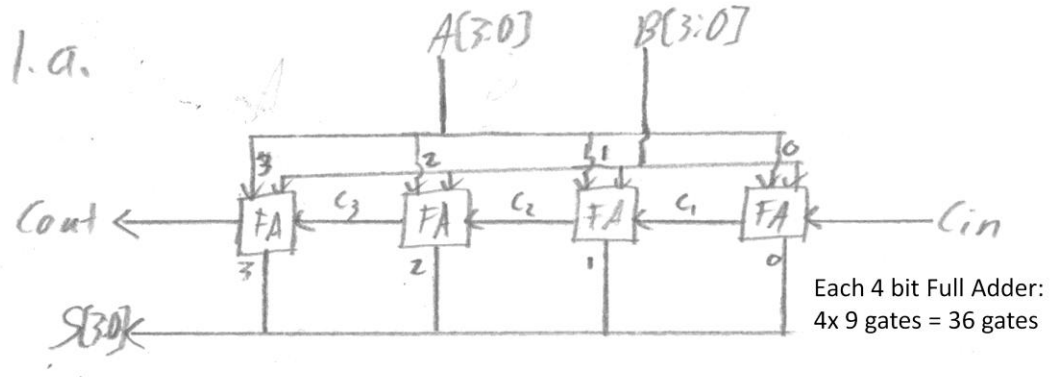
a. A 16 bit ripple carry adder.



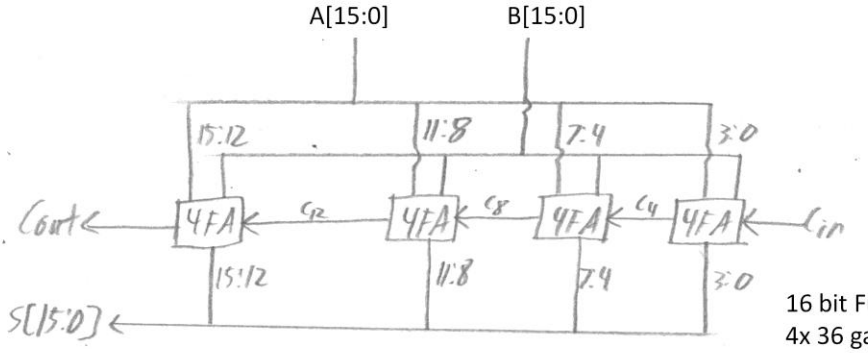
XOR



XOR has 3 2-input gates. 1-bit FA has 9 gates when not using P,G and the carry or 8 gates when using P,G but not the carry.



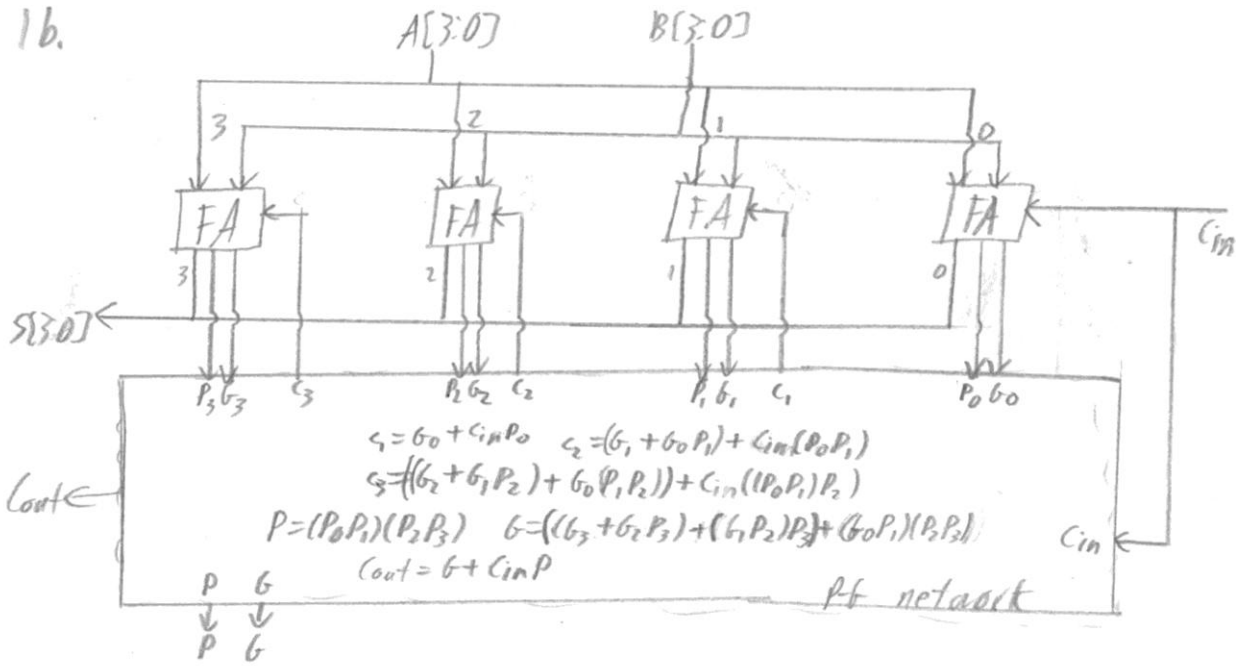
Each 4 bit Full Adder:
4x 9 gates = 36 gates



16 bit Full Adder:
4x 36 gates = 144 gates

Gate delay through first FA to carry out is 4 unit delays. Then 2 unit delays from carry in to carry out of the other FAs. Thus, first 4 bit FA has 4+2*3=10 delay. All others have 8 (just carry propagation). Therefore 16-bit FA has 10+8*3= **~34 unit delay**.

1b. A 16 bit carry look ahead adder.

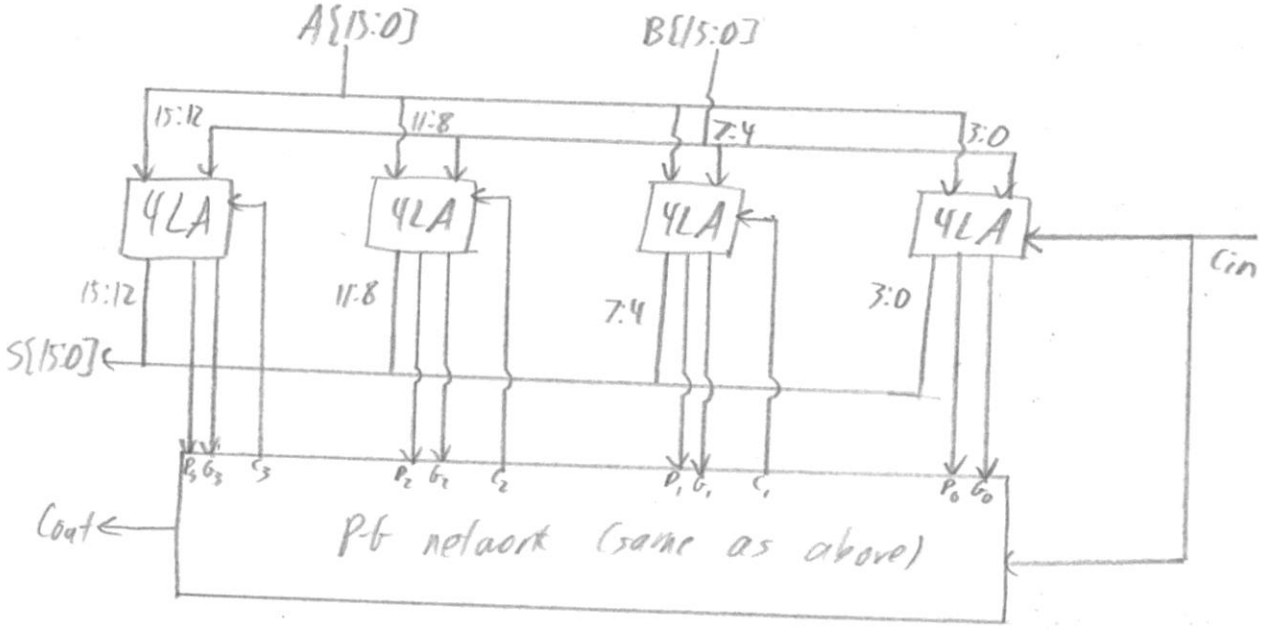


4x8 gates FA with P&G (no Cout from the 1 bit FA)	[32 gates]
C1 = G0 + CinP0	[2 gates]
C2 = G1 + C1P1 = G1 + P1G0 + CinP1P0 = (G1 + P1G0) + Cin(P1P0)	[5 gates]
C3 = G2 + P2C2 = G2 + P2G1 + P2P1C1 = G2 + P2G1 + P2P1G0 P P2P1P0Cin = ((G2 + G1P2) + G0(P1P2)) + Cin((P0P1)P2)	[9 gates]
P = (P0P1)(P2P3)	[3 gates]
G = G3 + G2P3 + G1P3P2+ G0P3P2P1 = ((G3 + G2P3) + (G1P2)P3) + (G0P1)(P2P3)	[9 gates]
Cout = G + CinP	[2 gates]

Total: 62 gates

Delays for 4 bit CLA:	{A,B} ➔ {Pi,Gi}	1 delay
	{A,B} ➔ P	3 delays
	{A,B} ➔ G	5 delays
	{P,G,Cin} ➔ Cout	2 delays

Thus for a single 4 bit CL adder, delay from Cin to Cout will be 6 unit delays.



For 16 bit adder, need 4X62 gates for each 4 bit block, then 30 for P-G network, Total = 278 gates.

After 1 delay, all FA P-G are settled. After 4 more delay, all 4LA P,G out are settled. Then, for the main P-G network, need another 2, 3, 4, and 4 delay for the C1, C2, C3, and Cout signals to settle. (Note that for highest level P-G block, C1 out is C4in for the [7:4] adder, C3 out is C12in for [15:12} adder.) Thus, highest 4LA will be the one on the critical path and have its C12in settle by delay 1+4+4=9. Need another 2 delays to generate C15in from C12in:

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[C15 = ((G2 + G1P2) + G0(P1P2)) + C12in((P0P1)P2)]
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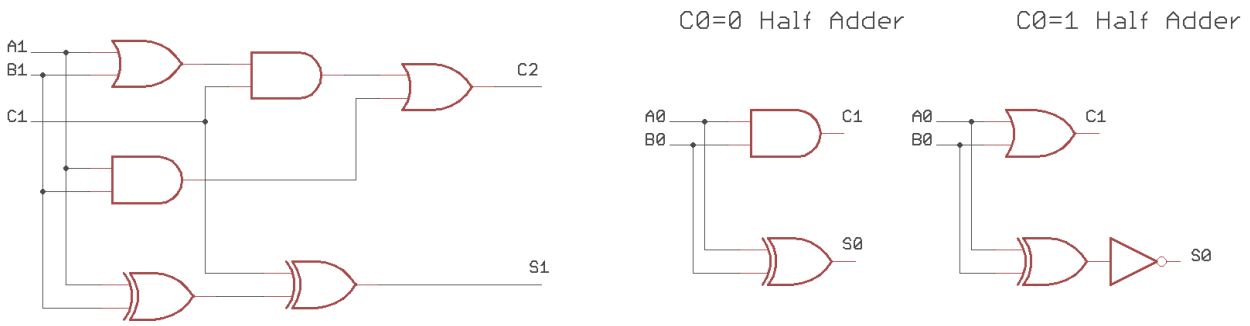
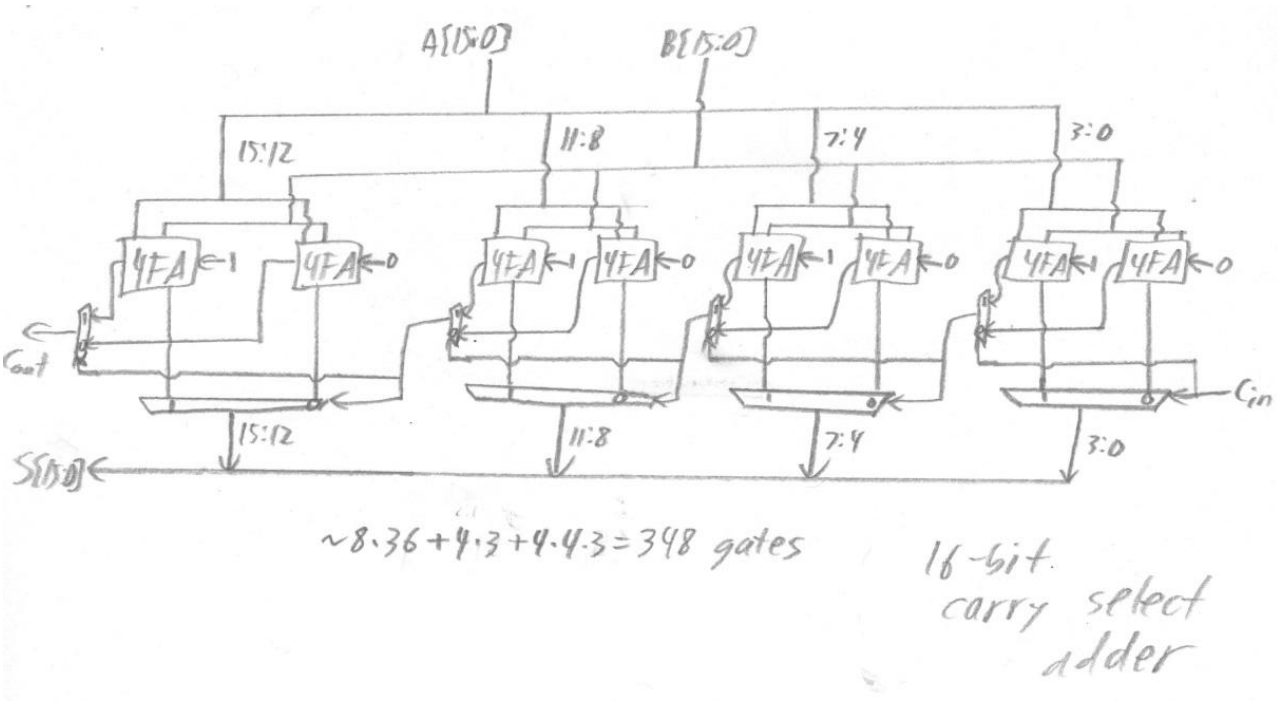
Inside the P-G network for the [15:12] 4LA block. And then 2 unit delays to incorporate the C15 carry input into the FA S[15] output. Thus, have a total of 9+2+2=**13 delay**.

1c. A 16 bit carry select adder.

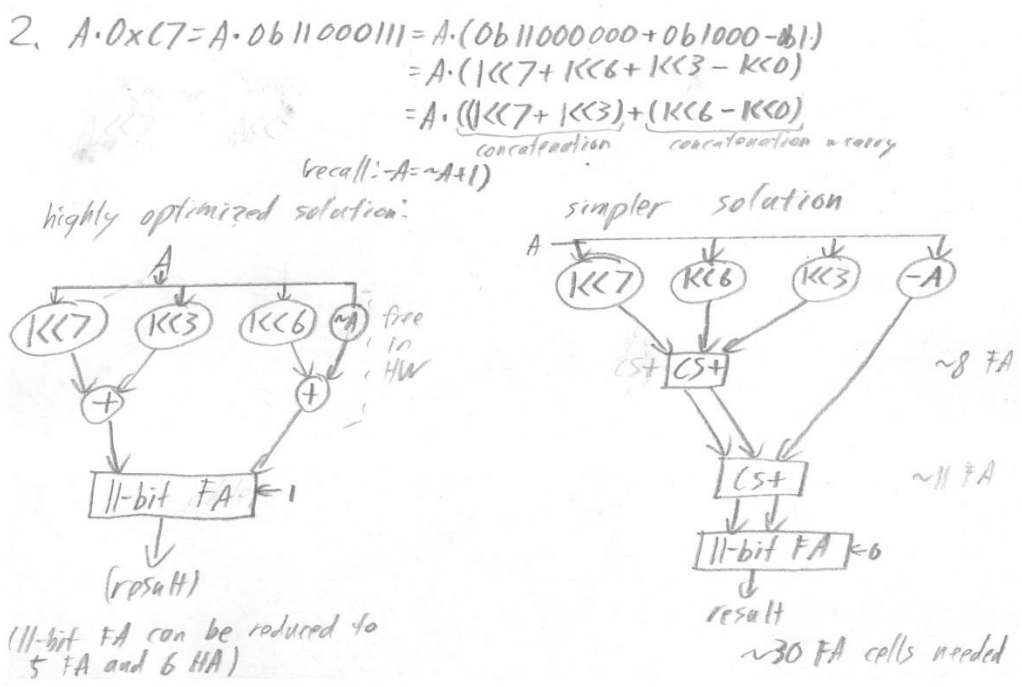
From part 1a, we had 10 unit delay from {A0,B0,Cin} to Cout, with 4 delays to first carry out, and 2 for each additional delay. If we consider two different 4 bit adders, one with Cin=0, and one with Cin=1, we can make it faster. Now first carry out will have one delay from {A0,B0}, so total will be 7 delays instead of 10.





Note, each 1-bit 2:1 mux requires 3 gates and has delay of 2. Also, note that if Cin is ready near beginning of cycle, can convert carry-select adder for bits 3:0 to ripple-carry adder and save 48 gates. Looking at carry propagation, need 10 delays for each FA to output a carry. Then, 8 delays for that carry to ripple through the muxes. Thus, this **requires 18 delay (16 if the lowest adder is simplified)**. If we use the FA optimized with carry in tied to zero or one, we have 7 adder delays + 2 mux delays to get C8 select + 2delays to get C12 select + 2 delays to get Cout select = 15 delays.

2. (35 pts) Multiplier
Design an unsigned combinational multiplier (no flip-flops or controller) for multiplying the unsigned constant value 199 = 0xC7 by the 4 bit variable Z[3:0]. Using only full-adder cells and inverters, draw a circuit that implements the multiplier using carry-save addition. Estimate delay from input to output. How many full-adder cells are needed?



Note that constant shifters just append 0s to the input value. Optimized solution has delay only associated with the 11-bit FA. From analysis in 1, this will have delay of around 4+2*10=**24 (if using ripple carry) or 13 (if using carry lookahead). For the simpler solution, each carry-save level adds about 4-gate delay (2 if willing to spend more area**).

Problem 3:

The charts with the logical values substituted in after interpreting the table and voltage specifications are as follows:

Determine the Boolean functions for the following:

a. Z.H = f(X.H, Y.H)

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

b. C.L = f(X.H, Y.H)

X	Y	C
0	0	0
0	1	1
1	0	1
1	1	1

c. C.L = f(A.L, B.L)

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

d. Z.H = f(X.H, A.L)

X	A	Z
0	1	1
0	0	0
1	1	0
1	0	0

Thus:

A. Z= !(X+Y)
B. C = X+Y
C. C = !(AB)
D. Z=(!X)A