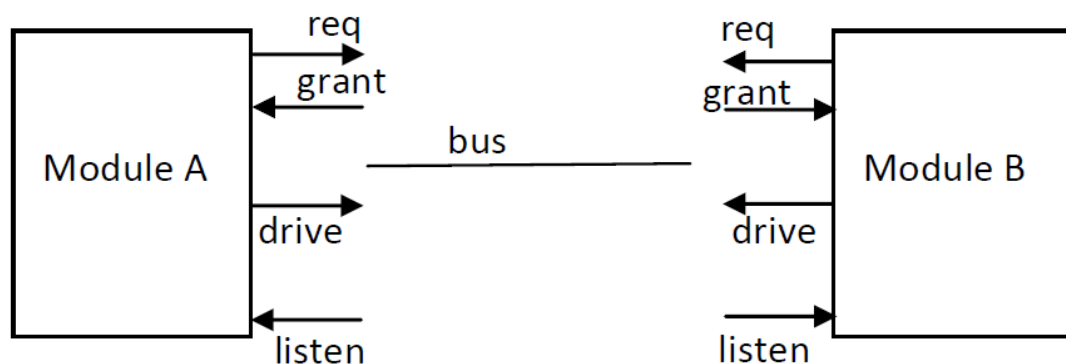


Midterm Review Question, Fall 2013 Update: * - very relevant, X - not relevant

1. Use NAND gate to implement a 2-to-1 mux. Then use hierarchical design to construct a 4-to-1 mux using the 2-to-1 mux.
2. Use 2-to-1 muxes to implement a 4 input NOR gate.
3. What is the number of rows in a truth table with N variables? How many different truth table can there be when there are N variables. If you are given LUTs with N/4 inputs, how many of those would you need to be able to implement all N-input functions?
- 4.* Given a 16 bit two input ALU which performs 8 types of operations, if you are to test it exhaustively, how many different input vectors do you need to supply?
- 5.X Use level-sensitive latches to implement a “register file” containing four elements, one read port and one write port. The input would be a clock signal, the address to the write port, the data to the write port, the address to the read port; the output would be the data for the read port. The behavior of the regfile should be the same as the one you have implemented in the lab.
- 6.* Write Verilog to design a FSM which controls a vending machine. The vending machine would dispense a can of coke if it receives 25 cents, and it does not give back changes. Besides clk and reset, there are three inputs to the vending machine: quarter, dime, nickel, which would be turned on high for 1 clk cycle if the corresponding coin is inserted. The FSM would produce 1 output, which is high for a cycle when 25 cents or more are received. You can assume only one of the three inputs would be high at a particular clock cycle.
7. Implement the function $\bar{a}\bar{b} + \bar{c} + \bar{d}$ using CMOS.
- 8.* Arbiter for bus communication: Two modules are communicating using a single bus. Each of them would output a “request” signal, and take in a “grant” signal. When the grant is low, the module would be listening on the bus, when the grant signal is high, the module would be driving the bus. Also, when one module finishes sending, it would deassert the request signal. Design a circuit using gates, registers and tristate buffers to coordinate the usage of the communication bus. Your circuit should only assert grant when modules assert request. When grant is given to one module, your circuit would wait for its request signal to go down before de-asserting the grant.



9.* What does the following testbench display? If the marked “=” is changed to “<=”, is there going to be any change in the produced output? Why or why not?

```

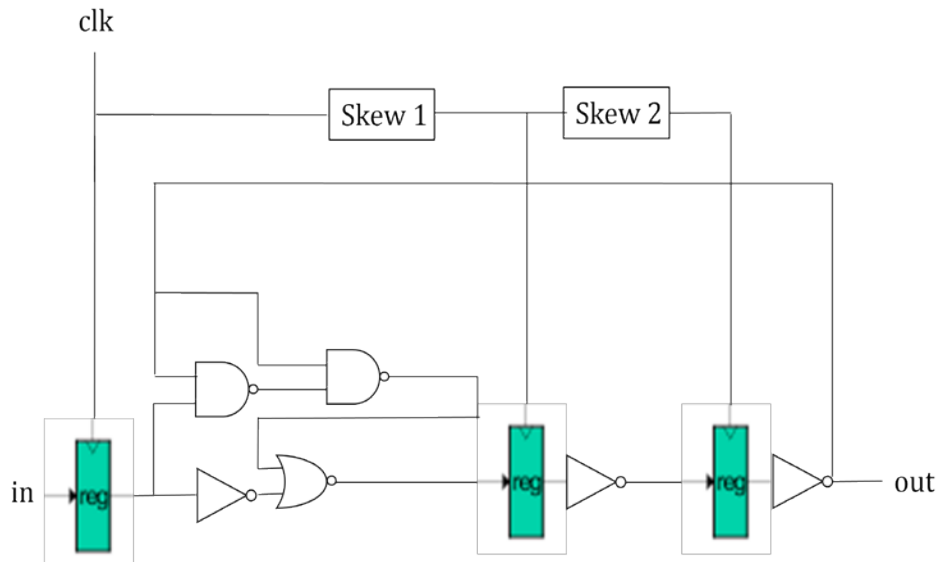
`timescale 1ns/1ps
module simme
reg[2:0] sig;

initial begin
#1sig=6;

initial begin
sig = 4;
#2;
repeat(3)
begin
$display("time = %d, sig = %d", $time, $sig);
#2 sig = sig+1;
end
end
initial begin
$monitor("monitor at time=%d: sig=%d", $time, $sig);
end
endmodule

```

10.* In the following circuit, each inverter has delay of 1ns, each two input gate has best case delay of 1ns and worst case delay of 2ns. Then for the registers, clock to q delay is 1 ns, setup time is 1 ns, hold time is 0.5 ns.



a) What is the maximum clock frequency if Skew 1=0 and Skew2=0.

- b) If we want to run the circuit at 100MHz, what is the acceptable range for Skew 1 and Skew 2? (You should consider both the upper bound and lower bound)

11.X You are given 2Kx64 RAM blocks. Create the datapath for a 4-way set associative 128KB cache with 32bit cache lines.

12.* Implement a FIFO with dual-port memory with asynchronous read and synchronous write. Your implementation should produce an “empty” and a “full” signal. You can assume the dimension of the memory matches with the FIFO.

13.* The pseudo-code for binary search is given below, where A is an array of n elements. The array is in ascending order

```
load n, load target
left=0;
index= -1;
right =n-1;
while(left<=right)
{
    mid = (right+left)/2;
    if(a[mid]<target)
        left = mid+1;
    else if(a[mid]>target)
        right = mid-1;
    else
    {
        index = mid;
        break;
    }
}
```

Let’s assume the array is stored in the memory location 0 to n-1, and the memory is a single ported memory with synchronous read. You are to design a datapath which performs binary search

- a. Write register transfer language description for the operations your circuit would need to perform.
- b. Given the following
 - i. Registers with reset and load-enable
 - ii. Greater than and less than comparators
 - iii. Addersdesign your circuit.