~7000 Lithium-Ion batteries in floorboard store 306 MJ of energy.

iPhone 5s: 23 KJ

Replacement price: $12,000

Apple’s cost: $4
200 KJ battery stores the energy of 1/2 a stick of dynamite.

If battery short-circuits, catastrophe is possible ...

The Watt: Unit of power. A rate of energy (J/s). A gas pump hose delivers 6 MW.

120 KW: The power delivered by a Tesla Supercharger. Tesla Model S has a 306 MJ battery (good for 265 miles).

1 J = 1 W s. 1 W = 1 J/s.
The same physics apply to an iPad mini retina (2013).

- 87 KJ battery.
- 10 J/s charger.
- 2.4 Hr charging time (in theory).

Data (Anandtech)
Sad fact: Computers turn electrical energy into heat. Computation is a byproduct.

Energy and Performance

Air or water carries heat away, or chip melts.
The Joule: Unit of energy. Can also be expressed as Watt-Seconds. Burning 1 Watt for 100 seconds uses 100 Watt-Seconds of energy.

1 Joule of Heat Energy per Second

1 Watt: Unit of power. The amount of energy burned in the resistor in 1 second.

1 Ohm Resistor

This is how electric tea pots work...

1 Joule heats 1 gram of water 0.24 degree C

20 W rating: Maximum power the package is able to transfer to the air. Exceed rating and resistor burns.
Cooling an iPod nano ...

Like resistor on last slide, iPod relies on passive transfer of heat from case to the air.

Why? Users don’t want fans in their pocket ...

To stay “cool to the touch” via passive cooling, power budget of 5 W.

If iPod nano used 5W all the time, its battery would last 15 minutes ...
Powering an iPod nano (2005 edition)

1.2 W-hour battery: Can supply 1.2 watts of power for 1 hour.

1.2 W-hr / 5 W ≈ 15 minutes.

More W-hours require bigger battery and thus bigger “form factor” — it wouldn’t be “nano” anymore :-().

Real specs for iPod nano:

14 hours for music,
4 hours for slide shows.

85 mW for music.
300 mW for slides.
Finding the (2005) iPod nano CPU ...

A close relative ...

Two 80 MHz CPUs. One CPU used for audio, one for slides.

Low-power ARM roughly 1 mW per MHz ... variable clock, sleep modes.

85 mW system power realistic ...
What's happened since 2005?

2010 nano
0.74 ounces
(50% of 2005 Nano)

“Up to” 24 hours audio playback.
70% improvement from 2005 nano.

0.39 W Hr
(33% of 2005 Nano)
0.44 ounce
0.19 W Hr

~0.6 ounce for frame
~0.3 ounce per lens
A clever prism projects a layer over reality light.
2.1 Wh battery - 5.3x as much energy as 2010 Nano.

Battery life very usage-dependent.

1.76 ounces - 2.4X the weight of 2010 Nano

640 x 360 Liquid Crystal on Silicon (LCoS) prism projector.

Logic Board
2011-class Smartphone (without a cellular radio)

16 GB Flash
1 GB DRAM

TI 4430 OMAP - 1 GHz dual-core ARM

Wi-Fi, Bluetooth

GPS
Desired screen size sets smartphone W x L

Depth? : Thin body vs. battery life

<table>
<thead>
<tr>
<th>Year</th>
<th>iPhone</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>iPhone</td>
<td>3.5&quot; TFT LCD, 480 x 320 pixels</td>
</tr>
<tr>
<td>2008</td>
<td>iPhone 3G</td>
<td>3.5&quot; TFT LCD, 480 x 320 pixels</td>
</tr>
<tr>
<td>2009</td>
<td>iPhone 3GS</td>
<td>3.5&quot; TFT LCD, 480 x 320 pixels</td>
</tr>
<tr>
<td>2010</td>
<td>iPhone 4</td>
<td>3.5&quot; IPS LCD, 960 x 640 Pixels</td>
</tr>
<tr>
<td>2011</td>
<td>iPhone 4 (CDMA)</td>
<td>3.5&quot; IPS LCD, 960 x 640 Pixels</td>
</tr>
</tbody>
</table>
### Battery Specifications

<table>
<thead>
<tr>
<th>Year</th>
<th>Model</th>
<th>Battery Type</th>
<th>Voltage</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>iPhone</td>
<td>Li-Ion Polymer, 3.7V</td>
<td>1170mAh</td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td>iPhone 3G</td>
<td>Li-Ion Polymer, 3.7V</td>
<td>1150mAh</td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>iPhone 3GS</td>
<td>Li-Ion Polymer, 3.7V</td>
<td>1220mAh</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>iPhone 4</td>
<td>Li-Ion Polymer, 3.7V</td>
<td>1420mAh</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>iPhone 4 (CDMA)</td>
<td>Li-Ion Polymer, 3.7V</td>
<td>1430mAh</td>
<td></td>
</tr>
</tbody>
</table>

- **38% gain in battery energy over 7 iterations**

- **iPhone 5s**: 23 KJ
<table>
<thead>
<tr>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
</tr>
<tr>
<td>2008</td>
</tr>
<tr>
<td>2009</td>
</tr>
<tr>
<td>2010</td>
</tr>
<tr>
<td>2011</td>
</tr>
<tr>
<td>iPhone</td>
</tr>
<tr>
<td>Li-Ion Polymer, 3.7V, 1170mAh</td>
</tr>
</tbody>
</table>

But thickness has decreased by 30% ...
iPhone
4, 4S, 5, 5S

Battery

L-shape
Main Board

Metal frame acts as antenna
In 7 years:

- 14x increase in transistor count
- 2.1x max clock speed increase
- Attached DRAM: 128 MB -> 1 GB
- 14x transistors: Dual CPUs, GPU, and to save energy.
Where's the DRAM?

“Package-in-Package”

512 MB SDRAM dies (2)

Apple A7 SoC

Dies connect using bond wires and solder balls ...
Apple A7
2013 SoC
iPhone/iPad

102 mm² die
28 nm CMOS
1.1B transistors

Dual-core
64-bit ARM
1.4 GHz

GPU fills 22% of die

200M transistors
4MB 6-T cells
**Performance:** Must be “close enough” to desktop performance ... most people no longer used a desktop (even in 2006).

**Size and Weight.** Ideal: paper notebook.

**Heat:** No longer “laptops” -- top may get “warm”, bottom “hot”. Quiet fans OK.
Battery: Set by size and weight limits ...

Battery rating: 55 W-hour.

At 2.3 GHz, Intel Core Duo CPU consumes 31 W running a heavy load - under 2 hours battery life! And, just for CPU!

At 1 GHz, CPU consumes 13 Watts. “Energy saver” option uses this mode ...

46x more energy than iPod nano battery. And iPod lets you listen to music for 14 hours!

Almost full 1 inch depth. Width and height set by available space, weight.
The CPU is only part of power budget!

2004-era notebook running a full workload.

“Other”

CPU

“Amdahl’s Law for Power”

If our CPU took no power at all to run, that would only double battery life!

Data courtesy Mahesri et al., U of Illinois, 2004
MacBook Air ... design the laptop like an iPod
2013 Air: 11.8 in x 7.56 in x 0.68 in; 2.38 lbs

2006 Macbook: 12.8 in x 8.9 in x 1 in; 5.2 lbs
Mainboard: fills about 25% of the laptop

39 W-h battery: 70% of 2006 MacBook’s 55 W-h
Servers: Total Cost of Ownership (TCO)

Machine rooms are expensive. Removing heat dictates how many servers to put in a machine room.

Electric bill adds up! Powering the servers + powering the air conditioners is a big part of TCO.

Reliability: running computers hot makes them fail more often.
Computations per W-h doubles every 1.6 years, going back to the first computer.

(Jonathan Koomey, Stanford).
Processors and Energy
Moore’s Law

curve shows transistor count doubling every two years

Transistor count

2 Thousand

1 Million

2.6 Billion
Main driver: device scaling ...

Every logic transition dissipates energy.

How can we limit switching energy?

1. Reduce # of clock transitions. But we have work to do ...
2. Reduce Vdd. But lowering Vdd limits the clock speed ...
3. Fewer circuits. But more transistors can do more work.
4. Reduce C per node. One reason why we scale processes.

Strong result: Independent of technology.

\[ E_{0\rightarrow1} = \frac{1}{2} CV_{dd}^2 \]
\[ E_{1\rightarrow0} = \frac{1}{2} CV_{dd}^2 \]
Dennard Scaling

Things we do: scale dimensions, doping, Vdd.

What we get: $\kappa^2$ as many transistors at the same power density!

Whose gates switch $\kappa$ times faster!

Power density scaling ended in 2003 (Pentium 4: 3.2GHz, 82W, 55M FETs). Why? We could no longer scale Vdd.

**TABLE I**

<table>
<thead>
<tr>
<th>Device or Circuit Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimension $t_{ox}, L, W$</td>
<td>1/$\kappa$</td>
</tr>
<tr>
<td>Doping concentration $N_a$</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Voltage $V$</td>
<td>1/$\kappa$</td>
</tr>
<tr>
<td>Current $I$</td>
<td>1/$\kappa$</td>
</tr>
<tr>
<td>Capacitance $\epsilon A/t$</td>
<td>1/$\kappa$</td>
</tr>
<tr>
<td>Delay time/circuit $VC/I$</td>
<td>1/$\kappa$</td>
</tr>
<tr>
<td>Power dissipation/circuit $VI$</td>
<td>1/$\kappa^2$</td>
</tr>
<tr>
<td>Power density $VI/A$</td>
<td>1</td>
</tr>
</tbody>
</table>
Scaling switching energy per gate ...

IC process scaling ("Moore's Law")

Due to reducing V and C (length and width of Cs decrease, but plate distance gets smaller).

Recent slope more shallow because V is being scaled less aggressively.

Leakage Currents slowed Vdd scaling

Even when a logic gate isn’t switching, it burns power.

\[ 0V = V_{IN} \]

\[ I_{Gate} \]

\[ I_{Sub} \]

\[ V_{OUT} \]

\[ C_L \]

\[ I_{Sub} \text{: Even when this nFet is off, it passes an Ioff leakage current.} \]

We can engineer any Ioff we like, but a lower Ioff also results in a lower Ion, and thus a lower maximum clock speed.

Igate: Ideal capacitors have zero DC current. But modern transistor gates are a few atoms thick, and are not ideal.

Intel’s 2006 processor designs, leakage vs switching power

A lot of work was done to get a ratio this good ... 50/50 is common.

Bill Holt, Intel, Hot Chips 17.
We can increase $I_{on}$ by raising $V_{dd}$ and/or lowering $V_t$.

$0.7 = V_{dd}$

$0.25 = V_t$

$1.2 \text{ mA} = I_{on}$

$I_{off} = 0$
We can decrease $I_{\text{off}}$ by raising $V_t$ - but that lowers $I_{\text{on}}$.

$I_{\text{off}} \approx 10 \text{ nA}$

$0.25 \approx V_t$

$1.2 \text{ mA} = I_{\text{on}}$

$0.7 = V_{dd}$
Device engineers trade speed and power

We can reduce $CV^2 (P_{active})$ by lowering $V_{dd}$.

We can increase speed by raising $V_{dd}$ and lowering $V_t$.

We can reduce leakage ($P_{standby}$) by raising $V_t$.

---

From: Silicon Device Scaling to the Sub-10-nm Regime
Meikei Ieong,¹ Bruce Doris,² Jakub Kedzierski,¹ Ken Rim,¹ Min Yang¹

CS 150 L24: Power and Energy
Tuesday, November 19, 13
Customize processes for product types ...

Transistor physics of leakage current ...

\[ \text{Vs} = 0V \quad \text{Vg} = 1V \quad \text{Vd} = 1V \]

\[ I \approx \mu A \]

The drain junction is also a capacitor, and puts negative charges in the substrate.

Away from the surface, the drain-induced charges remain even when the gate is off!

As we make L smaller, source and drain come closer, and \( I_{off} \) gets larger!
Solution concept: Fully-depleted channel

On:

\[ V_s = 0V \quad V_g = 1V \quad V_d = 1V \]

\[ I \approx \mu A \]

Off:

\[ V_s = 0V \quad V_g = 0V \quad V_d = 1V \]

\[ I \approx nA \]

We limit the depth of the channel so that the gate voltage “wins” over the drain voltage.

Done as shown, 5 to 7 nm depth for a 20 nm transistor. Requires expensive wafers

“FD-SOI” -- Fully-Depleted Silicon-On-Insulator
Transistor channel is a raised fin.
Gate controls channel from sides and top.
Channel depth is fin width.
12-15nm for L=22nm.
Thanks in large part to remarkable research started by Cal Berkeley professor Chenming Hu under a DARPA contract, the 20-nm process will likely be the last hurrah for the planar transistor (at least as we know it today), as the industry moves to FETs built with fins.

INS AND OUTS OF FINS

In a planar transistor of today, electrical current flows from source to drain through a flat, 2D horizontal channel underneath the gate. The gate voltage controls current flow through the channel. As transistor size shrinks with the introduction of each new silicon process, the planar transistor cannot adequately stop the flow of current when it is in an "off" state, which results in leakage and heat. In a FinFET MOSFET transistor, the gate wraps around the channel on three sides, giving the gate much better electrostatic control to stop the current when the transistor is in the "off" state. Superior gate control in turn allows designers to increase the current and switching speed and, thus, the performance of the IC.

Because the gate wraps around three sides of the fin-shaped channel, the FinFET is often called a 3D transistor (not to be confused with 3D ICs, like the Virtex-7 2000T, which Xilinx pioneered with its stacked-silicon technology).

In a three-dimensional transistor (see Figure 1b), gate control of the channel is on three sides rather than just one, as in conventional two-dimensional planar transistors (see Figure 1a). Even better channel control can be achieved with a thinner fin, or in the future with a gate-all-around structure where the channel will be enclosed by a gate on all sides.

The industry believes the 16-nm/14-nm FinFET process will enable a 50 percent performance increase at the same power as a device built at 28 nm. Alternatively, the FinFET device will consume 50 percent less power at the same performance. The performance-per-watt benefits added to the continued increases in capacity make FinFET processes extremely promising for devices at 16 or 14 nm and beyond.

That said, the cost and complexity of designing and manufacturing 3D transistors is going to be higher at least for the short term, as EDA companies figure out ways to adequately model the device characteristics of these new processes and augment their tools and flows to account for signal integrity, electromigration, width quantization, resistance and capacitance. This complexity makes designing ASICs and ASSPs even riskier and more expensive than before.

Xilinx, however, shields users from the manufacturing details. Customers can reap the benefits of increased performance per watt and Xilinx's Generation Ahead design flows to bring innovations based on the new UltraScale architecture to market faster.

Figure 1 – The position of the gate differs in the two-dimensional traditional planar transistor (a) vs. the three-dimensional FinFET transistor (b).
Sandy Bridge
32nm planar
1.16B transistors

Ivy Bridge
“Tick” 22nm FinFet
1.4B transistors

“Less than half the power @ same performance”
Leakage reduction in “Tock” 22nm Intel CPUs

Haswell (2013, 22nm FinFET)

Ivy Bridge (2012, 22nm FinFET)

—Cary Chin is director of marketing for low-power solutions at Synopsys.
Clock rates have flattened out, but ...

Between 1978 and 1986, the clock rate improved less than 15% per year while performance improved by 25% per year. During the "renaissance period" of 52% performance improvement per year between 1986 and 2003, clock rates shot up almost 40% per year. Since then, the clock rate has been nearly flat, growing at less than 1% per year, while single processor performance improved at less than 22% per year.
Performance: put more transistors to work

Figure 1.1 Growth in processor performance since the late 1970s. This chart plots performance relative to the VAX 11/780 as measured by the SPEC benchmarks (see Section 1.8). Prior to the mid-1980s, processor performance growth was largely technology driven and averaged about 25% per year. The increase in growth to about 52% since then is attributable to more advanced architectural and organizational ideas. By 2003, this growth led to a difference in performance of about a factor of 25 versus if we had continued at the 25% rate. Performance for floating-point-oriented calculations has increased even faster. Since 2003, the limits of power and available instruction-level parallelism have slowed uniprocessor performance, to no more than 22% per year, or about 5 times slower than had we continued at 52% per year. (The fastest SPEC performance since 2007 has had automatic parallelization turned on with increasing number of cores per chip each year, so uniprocessor speed is harder to gauge. These results are limited to single-socket systems to reduce the impact of automatic parallelization.) Figure 1.11 on page 24 shows the improvement in clock rates for these same three eras. Since SPEC has changed over the years, performance of newer machines is estimated by a scaling factor that relates the performance for two different versions of SPEC (e.g., SPEC89, SPEC92, SPEC95, SPEC2000, and SPEC2006).
Break
Five low-power design techniques

- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Clock gating
- Thermal management
Trading Hardware for Power

via Parallelism and Pipelining ...
Gate delay roughly linear with $V_{dd}$

And so, we can transform this:

Block processes stereo audio. 1/2 of clocks for "left", 1/2 for "right".

Into this:

Top block processes "left", bottom "right".

$P \sim \#\text{blks} \times F \times V_{dd}^2$

$P \sim 2 \times 1/2 \times 1/4 = 1/4$

CV$^2$ power only

---

THIS MAGIC TRICK BROUGHT TO YOU BY CORY HALL ...
### Power and Energy

#### Table 1: Power Normalization

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Power (normalized)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>1</td>
</tr>
<tr>
<td>Parallel</td>
<td>0.36</td>
</tr>
<tr>
<td>Pipelined</td>
<td>0.39</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>0.2</td>
</tr>
</tbody>
</table>

#### Table 2: Area Normalization

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Area (normalized)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
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</tr>
<tr>
<td>Parallel</td>
<td>3.4</td>
</tr>
<tr>
<td>Pipelined</td>
<td>1.3</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>3.7</td>
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</table>

#### Table 3: Voltage

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple</td>
<td>5V</td>
</tr>
<tr>
<td>Parallel</td>
<td>2.9V</td>
</tr>
<tr>
<td>Pipelined</td>
<td>2.9V</td>
</tr>
<tr>
<td>Pipelined-Parallel</td>
<td>2.0</td>
</tr>
</tbody>
</table>

---

**From:**

*Minimizing Power Consumption in CMOS Circuits*

Anantha P. Chandrakasan  
Robert W. Brodersen  
© Regents Fall 2013 © UCB
Multiple Cores for Low Power

Trade hardware for power, on a large scale ...
Cell:
The PS3 chip

IBM

PS

SONY

TOSHIBA

2006
Cell (PS3 Chip): 1 CPU + 8 “SPUs”

L2 Cache
512 KB

8 Synergistic Processing Units (SPUs)

PowerPC
One Synergistic Processing Unit (SPU)

SPU issues 2 inst/cycle (in order) to 7 execution units
256 KB Local Store, 128 128-bit Registers
SPU fills Local Store using DMA to DRAM and network
A “Schmoo” plot for a Cell SPU ...

The lower Vdd, the less dynamic energy consumption.

\[ E_{0 \rightarrow 1} = \frac{1}{2} C V_{dd}^2 \]

\[ E_{1 \rightarrow 0} = \frac{1}{2} C V_{dd}^2 \]

The lower Vdd, the longer the maximum clock period, the slower the clock frequency.

Failed
Clock speed alone doesn’t help E/op ...

But, lowering clock frequency while keeping voltage constant spreads the same amount of work over a longer time, so chip stays cooler ...

\[
E_{0->1} = \frac{1}{2} C V_{dd}^2 \quad E_{1->0} = \frac{1}{2} C V_{dd}^2
\]
Scaling V and f does lower energy/op

1 W to get 2.2 GHz performance. 26°C die temp.

7 W to reliably get 4.4 GHz performance. 47°C die temp.

If a program that needs a 4.4 GHz CPU can be recoded to use two 2.2 GHz CPUs ... big win.
How iPod nano 2005 puts its 2 cores to use ...

Two 80 MHz CPUs. Was used in several nano generations, with one CPU doing audio decoding, the other doing photos, etc.
**2013 Macbook Air**

Voltage range: 0.655V to 1.041V ... **2.5x** in $CV^2$ energy

---

### 13-inch MacBook Air (Mid 2013) CPU Comparison - Observed Voltages

<table>
<thead>
<tr>
<th></th>
<th>Idle</th>
<th>Cinebench 11.5 (1 thread)</th>
<th>Cinebench 11.5 (4 threads)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Core i5-4250U</td>
<td>0.665V (800MHz)</td>
<td>0.852V - 0.904V (2.3GHz - 2.6GHz*)</td>
<td>0.842V (2.3GHz)</td>
</tr>
<tr>
<td>Intel Core i7-4650U</td>
<td>0.655V (800MHz)</td>
<td>0.949V - 1.041V (2.9GHz - 3.3GHz*)</td>
<td>0.786V - 0.949V (2.8GHz - 2.9GHz*)</td>
</tr>
</tbody>
</table>

---

![Haswell CPU/GPU](image)
Powering down idle circuits
Add “sleep” transistors to logic ...

Example: Floating point unit logic.

When running fixed-point instructions, put logic “to sleep”.

+++ When “asleep”, leakage power is dramatically reduced.

--- Presence of sleep transistors slows down the clock rate when the logic block is in use.
Sleep Transistor Reduces SRAM Leakage Power

>3x SRAM leakage reduction on inactive blocks

A tiny current supplied in “sleep” maintains SRAM state.

Figure 4 – Intel® Atom™ Z2480 Processor SoC Block Diagram

CPU Power Management

The 32nm CPU in the Intel® Atom™ Processor Z2480 is a process-shrink of the original 45nm Atom™ micro-architecture [5]. The 32nm CPU doubled the size of the Gshare branch predictor to 8K entries and optimized memory copy performance. Additional low-power enhancements include operating the CPU at lower minimum voltage, reducing active power of the CPU PLL, separating voltage rails for CPU and the L2 cache, and enabling full power-gating of the CPU in the C6 standby mode. This section highlights the results of these low-power optimizations, and how they apply to smartphone use cases.

As shown in Figure 5, the Intel® Atom™ CPU provides a wide dynamic performance/power operating range. On Medfield, fine-grained active CPU power management is accomplished through dynamic frequency voltage scaling that is controlled by Enhanced Intel® SpeedStep® Technology [7], also known as CPU P-states. The dynamic range of the CPU ranges from 600MHz @ ~175mW to a sustained high frequency mode (HFM) of 1.3GHz @ ~500mW. For bursty workloads (e.g., interactive use of a web browser) the CPU can burst up to 2.0GHz @ ~1,200mW for short periods of time. As long as thermal headroom allows, the CPU can run in burst mode until thermal monitors in the platform, the SoC, or the CPU indicate that thermal design power limits have been reached. When this occurs, a combination of firmware and software throttle the CPU back into a lower P-state. Additionally, CPU w/512KB L2$
Intel Medfield
Switches 45 power “islands.”

Fine-grained control of leakage power, to track user activity.

“Race to idle” strategy -- finish tasks quickly, to get to power down.
Playing a game ...

Active system looks like this
Watching a video ...

CPU w/512KB L2$

Security Engine
Power Manager
Low Power Audio

Storage

CPU w/512KB L2$

2D/3D Graphics

Video Encode/Decode (1080p30)

Image Signal Processor

Display Controller (3 pipes)

CPU is now off!
Looking at phone screen, not doing anything ...

S0i1 – low activity

IEEE Micro Preprint
Phone in your pocket, waiting for a call ...

Standby State – just waiting for wakes
Slow down “slack paths”
Fact: Most logic on a chip is “too fast”

The critical path

Most wires have hundreds of picoseconds to spare.

Use several supply voltages on a chip ...

Why use multi-Vdd? We can reduce dynamic power by using low-power Vdd for logic off the critical path.

What if we can’t do a multi-Vdd design? In a multi-Vt process, we can reduce leakage power on the slow logic by using high-Vth transistors.

Logical partition into 0.8V and 1.0V nets done manually to meet 350 MHz spec (90nm).

Level-shifter insertion and placement done automatically.

Dynamic power in 0.8V section cut 50% below baseline.

Leakage power in 1.0V section cut 70% below baseline.

From a chapter from new book on ASIC design by Chinnery and Keutzer (UCB).
Gating clocks to save power
On a CPU, where does the power go?

Half of the power goes to latches (Flip-Flops).

Most of the time, the latches don’t change state.

So (gasp) gated clocks are a big win.
But, done with CAD tools in a disciplined way.

From: Bose, Martonosi, Brooks: Sigmetrics-2001 Tutorial
Synopsis Power Compiler can do this ...

"Up to 70% power savings at the block level, for applicable circuits"
Synopsis Data Sheet
Thermal Management
Keep chip cool to minimize leakage power

A recipe for thermal runaway

<table>
<thead>
<tr>
<th>Junction Temperature (T_J °C)</th>
<th>Normalized Static Power or I_{CCINTQ} Typical</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>1.00</td>
</tr>
<tr>
<td>50</td>
<td>1.46</td>
</tr>
<tr>
<td>85</td>
<td>2.50</td>
</tr>
<tr>
<td>100</td>
<td>3.14</td>
</tr>
</tbody>
</table>

Figure 3: $I_{CCINTQ}$ vs. Junction Temperature with Increase Relative to 25°C

Optimizing Designs for Power Consumption through Changes to the FPGA Environment

CS 150 L24: Power and Energy
IBM Power 4: How does die heat up?

4 dies on a multi-chip module

2 CPUs per die
115 Watts: Concentrated in “hot spots”

66.8°C == 152°F  
82°C == 179.6°F
Idea: Monitor temperature, servo clock speed

**Intel® Turbo Boost Technology 2.0 - Dynamic**

- **Max power**: 1.2-1.3X TDP
- **C0/P0 (Turbo)**
- **30-60 Sec**
- **5 Sec / 30-60 Sec exponential Average**
- **Buildup thermal budget during idle periods**
- **Sleep or Low power**
- **P > TDP**
- **Sustain power**
- **Time**

**Use accumulated energy budget to enhance user experience**

After idle periods, the system accumulates “energy budget” and can accommodate high power/performance for up to a minute.

In Steady State conditions the power stabilizes on TDP, possibly at higher than nominal frequency.

**TDP = Thermal Design Point**
Repeatedly running the same benchmark on all three products.

The TDP of each form factor dictates how long it can run at “top speed”

TDP = Thermal Design Point
Five low-power design techniques

- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Clock gating
- Thermal management
Return engagement for ... graphics chips

| Tue 12/3 | Lec #27: GPUs |