EECS150 - Digital Design
Lecture 20 –Timing Part 1

Nov. 5, 2013
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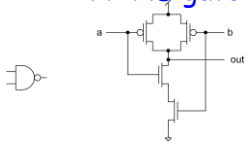
(slides courtesy of Prof. John Wawrzynek)

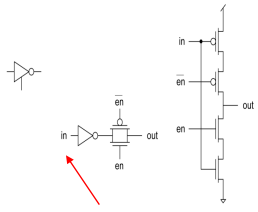
http://www-inst.eecs.berkeley.edu/~cs150

Recap and Outline

NAND gate:

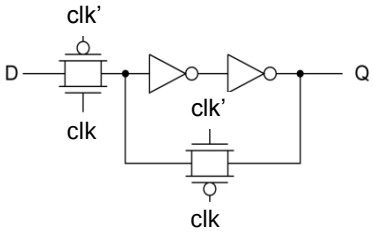


Tri-state buffer



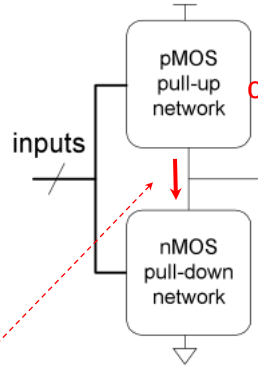
transmission gate useful in implementation

Latch Implementation:



Outline for Today
- Transmission gate, Latch
- CMOS delay

CMOS Logic Gates in General



Pull-up network conducts under conditions to generate a logic 1 output

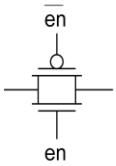
Pull-down network conducts for logic 0 output

Conductance must be mutually exclusive - else, short circuit!

Pull-up and pull-down networks are "topological duals"

Transmission Gate

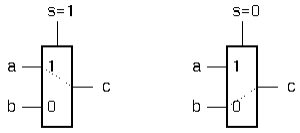
- Transmission gates are the way to build "switches" in CMOS.
- In general, both transistor types are needed:
  - nFET to pass zeros.
  - pFET to pass ones.
- The transmission gate is bi-directional (unlike logic gates).



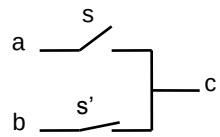
- Does not directly connect to Vdd and GND, but can be combined with logic gates or buffers to simplify many logic structures.

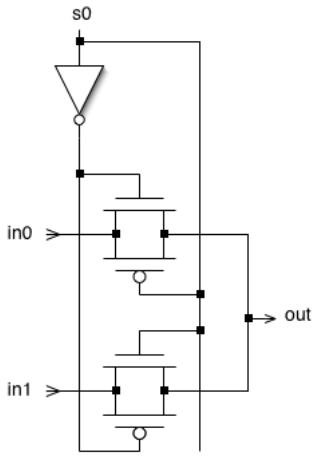
Transmission-gate Multiplexor

2-to-multiplexor:
$C = sa + s'b$



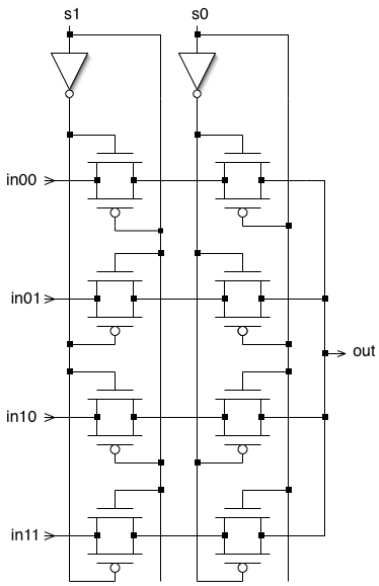
Switches simplify the implementation:





Compare the cost to logic gate implementation.

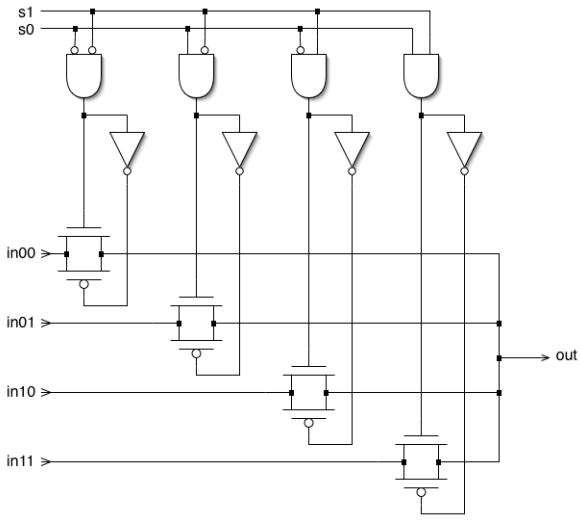
4-to-1 Transmission-gate Mux



- The series connection of pass-transistors in each branch effectively forms the AND of s1 and s0 (or their complement).
- Compare cost to logic gate implementation

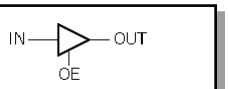
Alternative 4-to-1 Multiplexor

- This version has less delay from in to out.
- In both versions, care must be taken to avoid turning on multiple paths simultaneously (shorting together the inputs).



Tri-state Buffers

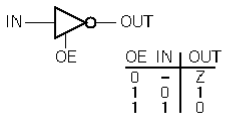
Tri-state Buffer:



OE	IN	OUT
0	0	Z
0	1	Z
1	0	0
1	1	1

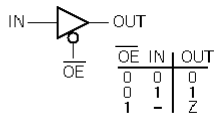
"high impedance"
(output disconnected)

Variations:



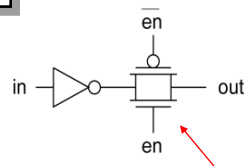
OE	IN	OUT
0	–	Z
1	0	1
1	1	0

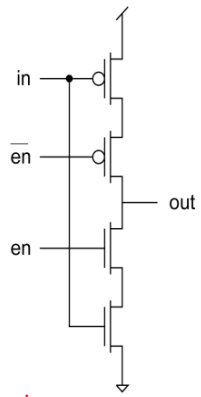
Inverting buffer



OE	IN	OUT
0	0	0
0	1	1
1	–	Z

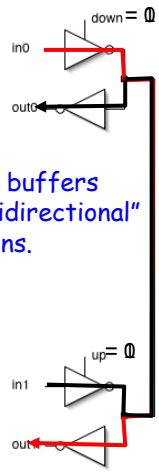
Inverted enable





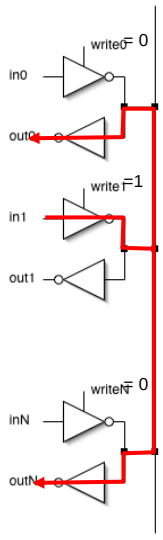
transmission gate useful in implementation

Tri-state Buffers



Tri-state buffers enable "bidirectional" connections.

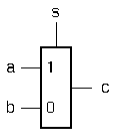
Tri-state buffers are used when multiple circuits all connect to a common wire. Only one circuit at a time is allowed to drive the bus. All others "disconnect" their outputs, but can "listen".



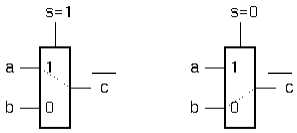
= 0

Tri-state Based Multiplexor

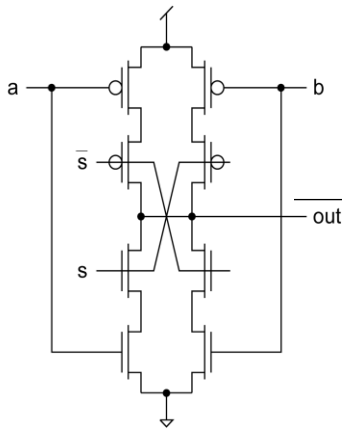
Multiplexor



If s=1 then c=a' (

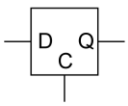


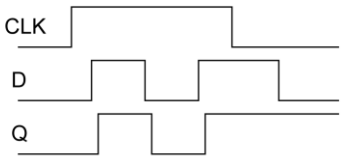
Transistor Circuit for inverting multiplexor:



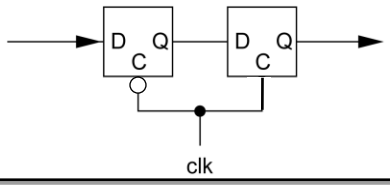
Latches and Flip-flops

Positive level-sensitive **latch**:

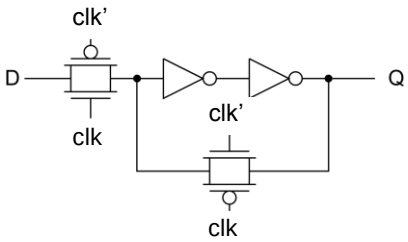




Positive Edge-triggered **flip-flop** built from two level-sensitive latches:



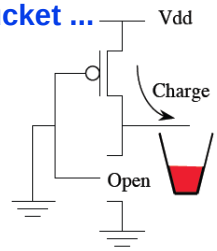
Latch Implementation:

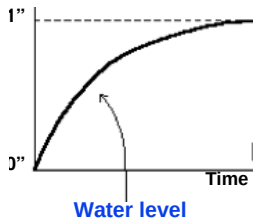


CMOS Delay: Transistors as water valves

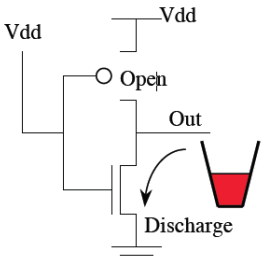
If electrons are water molecules, and a capacitor a bucket ...

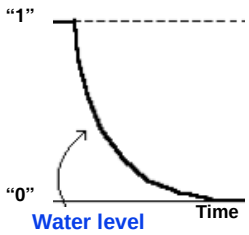
A "on" p-FET fills up the capacitor with charge.





A "on" n-FET empties the bucket.

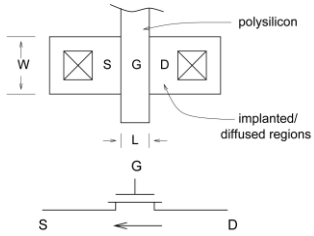




This model is often good enough

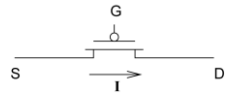
Transistors as Conductors

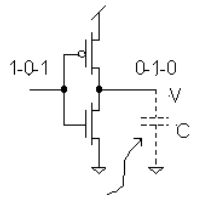
- Improved Transistor Model:
  nFET



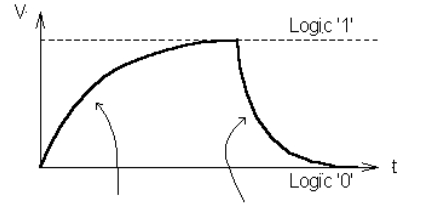
- We refer to transistor "strength" as the amount of current that flows for a given Vds and Vgs.
- The strength is linearly proportional to the ratio of W/L.

pFET





Models inputs to other gates & wire capacitance

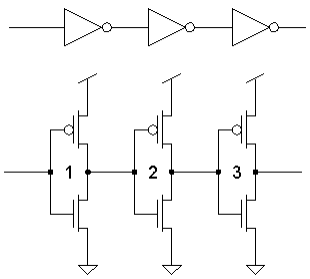


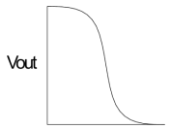
rate dependent on pullup strength & C

rate dependent on pulldown strength & C

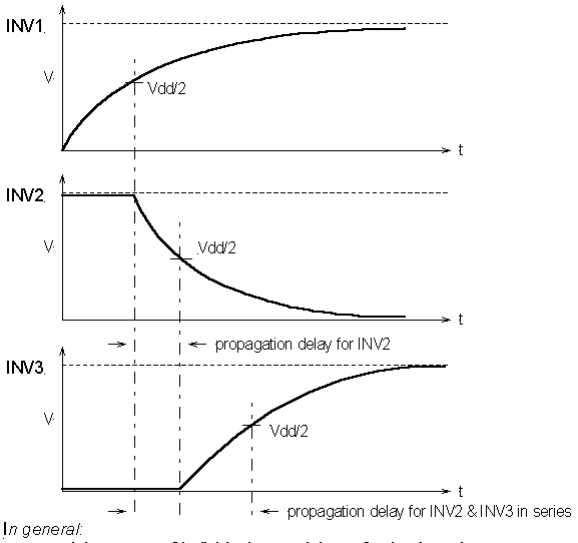
Gate Delay is the Result of Cascading

- Cascaded gates:



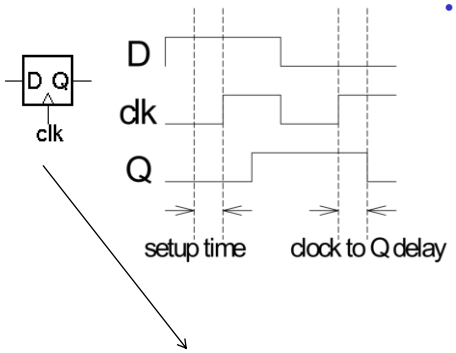


"transfer curve" for inverter.

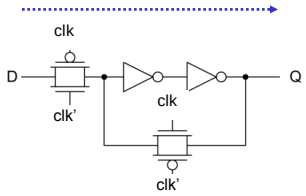


In general:
prop. delay = sum of individual prop. delays of gates in series.

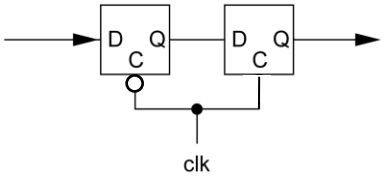
Delay in Flip-flops

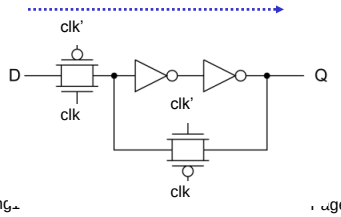


- Setup time results from delay through *first* latch.

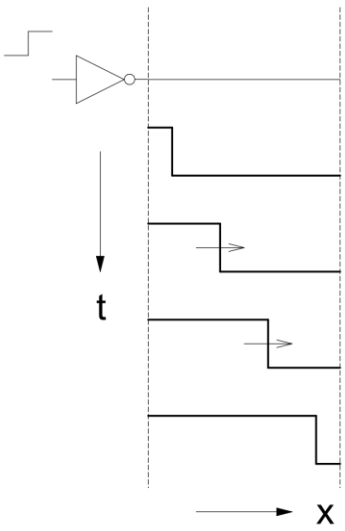


Clock to Q delay results from delay through *second* latch.





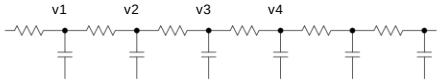
Wire Delay



- Ideally, wires behave as "transmission lines":
  - signal wave-front moves close to the speed of light
    - ~1ft/ns
  - Time from source to destination is called the "transit time".
  - In ICs most wires are short, and the transit times are relatively short compared to the clock period and can be ignored.
  - Not so on PC boards.

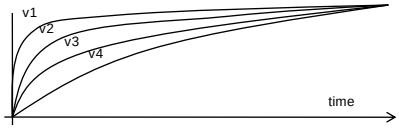
Wire Delay

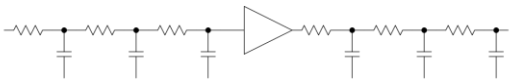
- Even in those cases where the transmission line effect is negligible:
  - Wires posses distributed resistance and capacitance



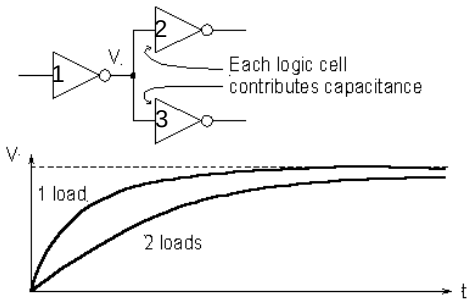
  - Time constant associated with distributed RC is proportional to the *square* of the length

- For **short wires** on ICs, resistance is insignificant (relative to effective R of transistors), but C is important.
  - Typically around half of C of gate load is in the wires.
- For **long wires** on ICs:
  - busses, clock lines, global control signal, etc.
  - Resistance is significant, therefore distributed RC effect dominates.
  - signals are typically "rebuffered" to reduce delay:



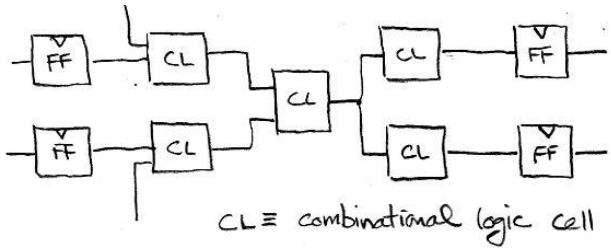


Delay and "Fan-out"



- The delay of a gate is proportional to its output capacitance. Connecting the output of gate to more than one other gate increases it's output capacitance. It takes increasingly longer for the output of a gate to reach the switching threshold of the gates it drives as we add more output connections.
- Driving wires also contributes to fan-out delay.
- What can be done to remedy this problem in large fan-out situations?

Components of Path Delay



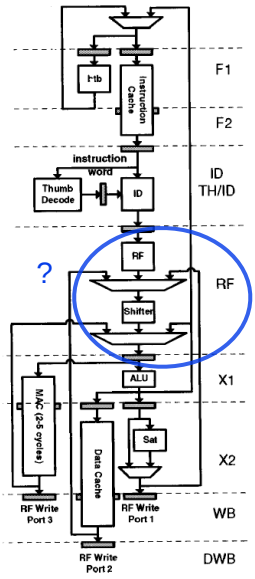
1. # of levels of logic
2. Internal cell delay
3. wire delay
4. cell input capacitance
5. cell fanout
6. cell output drive strength

Who controls the delay?

got here

	Silicon foundary engineer	Cell Library Developer, FPGA-chip designer	CAD Tools (logic synthesis, place and route	Designer (you)
1. # of levels			synthesis	RTL
2. Internal cell delay	physical parameters	cell topology, trans sizing	cell selection	
3. Wire delay	physical parameters		place & route	layout generator
4. Cell input capacitance	physical parameters	cell topology, trans sizing	cell selection	
5. Cell fanout			synthesis	RTL
6. Cell drive strength	physical parameters	transistor sizing	cell selection	instantiation (ASIC)

Searching for processor critical path



Must consider all connected register pairs, paths from input to register, register to output. Don't forget the controller.

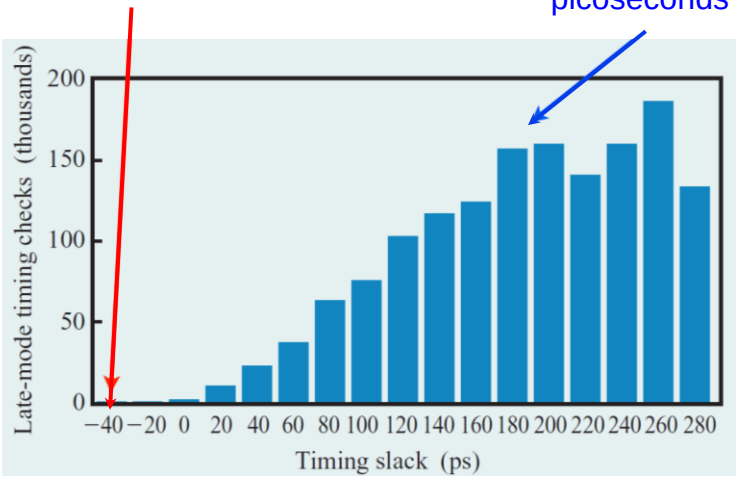
- Design tools help in the search.
  - Synthesis tools report delays on paths,
  - Special static timing analyzers accept a design netlist and report path delays,
  - and, of course, simulators can be used to determine timing performance.

Tools that are expected to do something about the timing behavior (such as synthesizers), also include provisions for specifying input arrival times (relative to the clock), and output requirements (set-up times of next stage).

Real Stuff: Timing Analysis

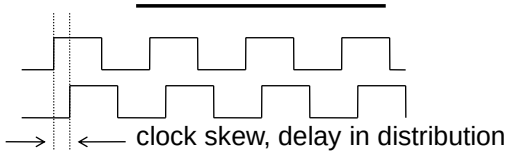
The critical path

Most paths have hundreds of picoseconds to spare.



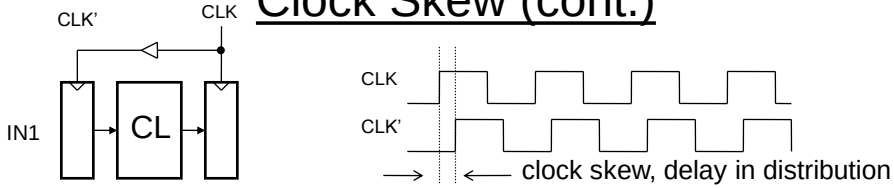
From "The circuit and physical design of the POWER4 microprocessor", IBM J Res and Dev, 46:1, Jan 2002, J.D. Warnock et al.

Clock Skew



- Unequal delay in distribution of the clock signal to various parts of a circuit:
  - if not accounted for, can lead to erroneous behavior.
  - Comes about if:
    - clock wires have different delay,
    - circuit is designed with a different number of clock buffers from the clock source to the various clock loads, or
    - buffers have unequal delay.
  - All synchronous circuits experience some clock skew:
    - more of an issue for high-performance designs operating with very little extra time per clock cycle.

Clock Skew (cont.)

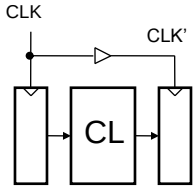


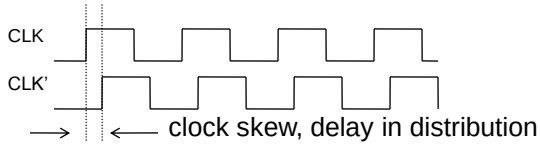
- If clock period $T = T_{CL}+T_{setup}+T_{clk->Q}$, circuit will fail.
- Therefore:
  1. Control clock skew

     a) Careful clock distribution. Equalize path delay from clock source to all clock loads by controlling wires delay and buffer delay.

     b) don't "gate" clocks in a non-uniform way.
  2. $T >= T_{CL}+T_{setup}+T_{clk->Q}$ + worst case skew. (setup time violation)
  3. Watch out for hold time violation (inputs from NSD change before clock)
- Most modern large high-performance chips (microprocessors) control end to end clock skew to a small fraction of the clock period.

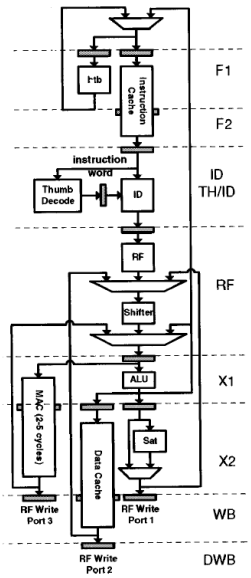
Clock Skew (cont.)

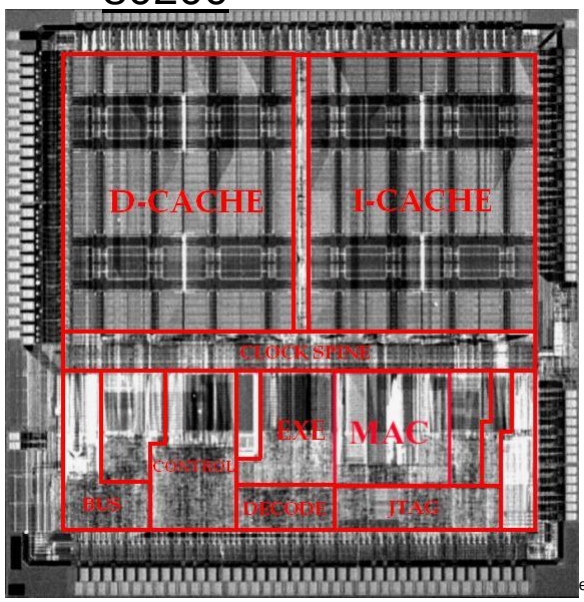




- Note reversed buffer.
- In this case, clock skew actually provides *extra time* (adds to the effective clock period).
- **Watch out for hold time violation!** WB
- This effect has been used to help run circuits as higher clock rates. Risky business!

Real Stuff: Floorplanning Intel XScale 80200





Conclusions

- CMOS details – transmission gate, latch
- timing
- PLL