Homework 4 v1.0
EECS150, Fall 2012
Due Friday, 6 pm, Sept 21, outside 125 Cory

1. How many CLBs do you need to implement an FSM with 10 state bits, each one driven by an arbitrary function of 11 variables each?
2. In registered mode, the D input of each FlipFlop on the ATF16V8 can take in the OR or NOR of the product (AND) of any combination of the 8 inputs and 8 state bits (Figure 11-1). Give an example of a logic function of those 16 inputs that can NOT be implemented in this way.
3. You are helping a graduate student design a board to test her new CMOS communications chip. Given an 80MHz clock source, use the Atmel ATF16V8 registered PAL to generate a four-phase non-overlapping clock. Each phase should be true for approximately 12ns every 100ns, and no two phases should be true at the same time.
    a. Show your state transition diagram, state transition function, and output function
    b. Define which pins on the Atmel chip will represent which states and outputs, and how the "OUTPUT LOGIC" block will be configured for each.
    c. Fill in the fuse table with a dot on each intersection where you want a connection.
4. The board works, and now her professor demands that she do bit error rate testing. She would normally use an expensive programmable pseudo-random bit generator, but one of the other grad students broke it, and her advisor is too cheap to buy a new one for $50k. She needs a 10Mbps pseudo-random sequence. You tell her "I can make you one with my Atmel registered PAL for under $5!"
    a. Explain how you will do it by drawing the logic that you will implement (you don't need to fill in the fuse table).
    b. If she needs at least 60,000 pseudo-random bits before the sequence repeats, how would you change your design?
5. Use Karnaugh maps to find a minimal sum-of-products expression for the function given in:
    a. The truth table in Figure 2.84
    b. Interview question 2.2 (page 100).
6. Question 3 from Midterm 2, fall 2006 (available from HKN website: https://hkn.eecs.berkeley.edu/examfiles/cs150_fa06_mt2.pdf)