Homework 2
EECS150, Fall 2012
Due Friday, 6 pm, Sept 7, outside 125 Cory

1. DDCA 4.{46, 47, 48}

2. At Golden Bear Circuits you have designed a new washing machine controller circuit using your ML505 development board. You figure out that you can fit the whole circuit in a $10 FPGA. If you make it in 180nm CMOS it will take 5mm2 of CMOS area. If you make it in 22nm CMOS it will take 0.5mm2 of die area. The cost to design and test a board with the FPGA is $50k. Suppose the cost for all of the masks for 180nm CMOS is $250k, and $10M for 22nm CMOS. Assume that the yielded (tested) cost per square millimeter is $0.05 for 180nm CMOS, and $0.10 for 22nm CMOS. Your boss asks you which of the three technologies you should use to make your product.
    a. What is the variable cost (the per-part cost) of each approach?
    b. What is the total cost of the very first part you make in each technology, if you only make 1?
    c. What is the total amortized cost per part (total cost divided by total number made) in each technology assuming that you make one thousand, one million, or one billion?
    d. What is the minimum number that you need to sell in order to justify using the 180nm process?
    e. What is the minimum number that you need to sell in order to justify using the 22nm process?

3. Design a 3 bit counter with 2 inputs, *up2* and *down3*, and 2 outputs, *even* and *prime*. The counter should reset to state 5. If both up2 and down3 are asserted, the counter should count down by 1, if neither is asserted it should count up by 1. If either one is asserted alone it should count according to the name of the input (up by twos, down by threes).
    a. Draw the state transition diagram.
    b. Draw a high-level block diagram of the counter, with blocks of the state, state transition function, and output function (you don't need to fill in detail).
    c. Write the Verilog that will implement the counter.

4. Wikipedia has an example of a 3 tap FIR filter for calculating a moving average http://en.wikipedia.org/wiki/Finite_impulse_response. Assuming that you have a 16 bit ADC running at 44.1kHz (CD rate) and you have a clock signal CLK at 16*44.1kHz, design a 4 tap moving average filter to smooth the audio signal.
    a. Draw the block diagram of your solution. Do you need a multiplier? How will you do "division"? Make sure that you show how many bits are in each bus.
    b. Implement your filter in verilog.