Reading 8.5 Mem mapped I/O

Draw Foll
Add 2 pipeline regs
Label all lines (W/stage, MemWrite, MemWrite, MemWrite)
print
run inst. segment e.g. 7, 99, 51, 54

For add (and all R-type) result is ready at end of cycle 2
Q: Why not write it on the next reg else?
A: Look at prev. LW example. Both LW & ADD would meet at same time.
Q: What if you could? Any power, execution?
A: No, 1 cycle/mis
5.8 Strings & the stack

$sp = 0xFFFF FFFC

$sp = 0x1000 8000

$sp = 0x4000 0000

0x0000 0000

\text{mem map}

\text{not quite enough, reads trigger later too}

\text{DEC}

A: read RX dat

B: set TX busy

\text{UART}

\text{DataIn}

\text{DataIn Valid}

\text{Data Out Ready}