partners - another class

Verilog, testbenches in 7.6 on web?

Hazards, delay slot, stalls

3 stage pipeline

<table>
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<tr>
<th>DEC</th>
<th>IM</th>
<th>RF</th>
<th>ALU</th>
<th>DM</th>
<th>RF</th>
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</table>

How to do 3-stage pipeline?
Must be compatible w/ compilers

Compilers will add a delay slot on all
J*, B*, LB, LH, LW (Table 1)

- expects this command to be executed!
- can't optimize away the delay slot!

Compiler will add hop if all else fails

Why are delay slots there?
- improved performance ~1/2 the time.
- alternate stall (avoid stall)

Stalls:
- required on 5-stage even w/ fast
  1-men, d-men
- not required or allowed on 3-stage
  until we use caches/DRAM
3 stage
PC, Im, REG | ALU | DM, WB, RF

N.B. I-mem, D-mem are synch read/Write.
their input address for reads is a
regdest

I-mem

D-mem - part of pipeline register

I-mem is also dual
ported so that you
can write to it from
data path
BIOS = loader

separate Im, ALU, DM
draw visio of clear pipeline register
labels
write down all 32 segment from book
show exactly what's on which line

define blocks, unit test!
Data Bypasser

Fig 7.51

1W $50, 40($0) IM
and $t0, $50, $51
or $t1, $54, $50
sub $t2, $50, $55

0 = 50 needed

1W $50 IM\[RF\]
and $t0, $50 IM\[RF\]
or $t1, $50 IM\[RF\]
sub $t2, $50 IM\[RF\]

4th available

stable

written

[ALU] [DM] [RFw]

↓ impossible. Must stall (or double talk)

← forward. ALU need data from Result Word

← no problem

3 stage

IM [RF] [ALU] [DM, RFw]

↓ stable

written

solution #1 = stall NO!

#2. delay slot. compiler fill it up

↓ impossible.

this one works out better if RFw is in the 2nd stage.
Data hazards Fig 7.49
1st write stable written

add $s0, $i, $r0
   In  |  RF  |  ALU  |  DR  |  RF  |  WR

and $t0, $s0
   In  |  RF  |  ALU

or $t1, $s0
   In  |  RF  |  ALU

sll $t2, $s0
   In  |  RF  |  0

Control hazard Fig 7.54
3 stage

20 BEQ $t1, $t2 40 JUMP
24 AND
28

which one?
64

use mux

inst 24 always executed (branch delay slot)
no flush needed

3 stage

add $s0, $i, $r0
   In  |  RF  |  ALU  |  DR  |  RF  |  WR

and $t0, $s0
   In  |  RF  |  ALU

or $t1, $