Serial in - parallel out (SISO)

Pipelining: 3.5
Micro MIPS: 65

Delay: 2 ns
Micro pipeline: 2.5

Critical path: 2 ns
f = 500 MHz

Pipeline: (A + B) * C + D
T_{pk} = 2 ns
f = 250 MHz

Multiplier is a long sequence of adders.
Branch is half

critical path: f_{max} = 1000 MHz

What about register cost?

Overall critical path less or shorter?
Timing (3.5 ns)

$t_{ceq}$ - clock to Q contamination
outputs will be stable at prev value
at least this long (min)

$t_{pd}$ - clock to Q propagation
new value will be stable
after this time (max)

must have

$T_c = t_{ceq} + t_{pd} + t_{setup}$

given $t_{ceq}$ & a FF, max & delays

$t_{pd} = T_c - (t_{ceq} + t_{setup})$

$\frac{1}{F}$ cost of FF

0.4 ns

Block RAM clock period ~ 2 ns
Clock jitter ~ 0.2 ns
Hazard - risk depends on results of audits, not that it's not unrelated.

Data - repetit, value not written yet, content - isn't as known yet.

<table>
<thead>
<tr>
<th></th>
<th>F</th>
<th>D</th>
<th>E</th>
<th>M</th>
<th>W</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A role on RF needs a reminder

"1st half" "2nd half"

Is just a way to take what people click

- Forwarding

1. Add $50...
2. Add $51, $50...
3. And $60, $50...

7 to 48
need stable signal to hold latches, so

\[
t_{ccg} + t_{pd} > t_{hold}
\]

t_{pd} could be 0

t_{hold} < t_{ccg}

CLK

\[
D \quad X \quad Y \quad Z \quad Q
\]

\[
t_{ccg} \xrightarrow{2\ t_{inv}}
\]

\[
t_{setup} = \text{propagation } D \rightarrow X \rightarrow Y
\approx 2 \text{ inverters}
\]

\[
t_{hold} \approx \text{12\ inverters}
\text{often 0}
\]

\[
Pipelined
\]

\[
\text{Critical Path: LW}
\]

\[
T_c = t_{ccg} + t_{nom} + t_{read} + t_{mux} + t_{alu} + t_{mem} + t_{mux}
\]

\[
(9C) \quad I \quad RF \quad ALU \quad MEM
\]

\[
= t_{ccg} + t_{sety} + 2t_{nom} + t_{alu} + t_{read} + 2t_{mux}
\]

\[
\text{Yuk.}
\]