This week Friday 3

CLB
SAR
16-nm

Last time

$17 \Rightarrow D \Rightarrow \overline{D} \Rightarrow \text{shift reg}$

- configurable logic
- all controlled by configurable interconnect
- 1 read, 5 shift reg
- configurable I/O

---

4 inputs

- configurable logic
- 2 slices = 1 CLB

$160 \times 54 \text{ CLBs} = 8,640$

~ 70,000 (6-LUT + DFF)

---

2 7-inputs + 1 8-input

- ripple-carry half

- and DSP 48E Slices (64 of them)

~ 248 slice ALUs
SAR ADC
- example of mixed analog/digital design
- good analog design, need to have some digital
- good example of real-world application

Simple linear scale
1 - 1024 cycles

Binary search
1023
512
0

DAC

S/H

not 0.150

State diagram

1024 x 2 state line FF
But logic for state transition will involve 11 variables.

TB, d9...d0

2 hard to draw (understand)

factor into 2 separate statements

14 FF

Much simpler logic - counter

Or use shift register, not counter

\[ \text{resb} \]

LD

SH

[1111]18(TB)

[1111]
Back to chapter 2

de Morgan's
\[ \overline{A + B} = \overline{A} \cdot \overline{B} \]
\[ A + B = \overline{A \cdot B} \]

\[ F = \sum_i A_i \]
\[ Y = \prod_i A_i \]
\[ Y = F = \sum_i \overline{A_i} \]

Bubble pushing.
\[ \text{Do} \iff \text{g} \]
\[ \text{Do} \iff \text{g} \]

\[ \text{NOR} / \text{NOR} / \text{INV} ? \]

Who cares?

\[ T \]

\[ A_0 \rightarrow \overline{A_i} \rightarrow \cdots \rightarrow A_n \]

\[ \text{nor}(A_i) \]

\[ \text{NOR} / \text{INV} \]

\[ \text{SOI with dedicated input} \]

\[ \phi : \text{föze, anti-föze, mask-programmed, FF controlled, double gate} \]