Reading 3.5.1-4.3
3.4 Moore only
sp. lectures
(ch 7)
H2 prob 2

#2

C(150 12FA W3LZ)

= 1

= 1

#display
#monitor"prints to console whenever inputs change

= x3 * 1'b2

Initial CLK = 0;
Always #HALF t

Param Clock

= 0

= 0

0 15 20

time scale 1ns/ps
units of # in sim.

assign # = # delay

= $delay

Synthetic vs. test bench

= Re-read 4.8
2 testbench files
   - random + hard coded
   - input file
both create a clock
instance ALU, ALU dec or DUTs
use task check output
use system task $display
ove for loops

in industry often write the interface spec, then testbench, then module. why?
Example 3.13

Figure showing a digital circuit with a D flip-flop and other components connected with clock signals (CLK).

Description:
- The figure illustrates a digital circuit with a D flip-flop labeled as "D" connected with clock signals (CLK).
- The flip-flop is used to shift register bits.
- There is a note indicating that the shift register can be big and has scan chains for testing.
- The circuit includes logic gates and connections labeled with variables and conditions.

Additional Elements:
- Diagrams of other digital components and logic gates are present, illustrating various logic functions and connections.

Overall, the page contains detailed schematics and explanations related to digital circuitry and testing techniques.
Slightly different from ALUop in book

1) Need to understand how MIPS works
2) Piazza