pad ring, saw kerf
200 um
pads on 100 um centers

floor plan
RAM
ROM
Flash
DRAM
cache

external DRAM = $1 ?

SDRAM - design a
32b, 8 row, 32 x 1, burst length 2

50% fabric

yielded, tested die cost ~ 10k/mm^2

Cost model
Masks
Flash
Dram
SRAM
logic
90k
1.4
100k
50k

ROM
104 k/mm^2
Addressing

MIPS pixels

0.0 in frame 0x10400000

Y x 21300

w 48

106 10 10

bottom 3 bytes

CMD pixels

0x0xxxx xy

MIPS pixels

16'b x, 10'b y, 2'b 0

SDRAM pixels

6/3 bit core, 6/3 frame, 10/3 y, 9/6 x[9:1]

returns 8 pixels

aligned on even pixel boundary (64'b read)
6-6-6-22

6-6-6-22

out memory
200mhz 3-3-3-8
as implemented 5-3-3-8

T_{CL} = 5 + T_{AC} = 25ns

Burst 1
Row

t_{RP}

Pre

ACT

READ

t_{RC}

CAS

t_{CAS}

RAS-CAS

t_{RAS}

t_{RP}

t_{RP}

t_{RC}

TRAS

t_{RC}

t_{RC}

t_{RAS}

t_{RAS}

t_{RAS}

t_{RP}

time to read first bit w/ addressing

1st by w/ wrong row or not

act only w/ wrong row ACT

TRAS T_{RP}