11/13/15 W13
11/20 W14 CPUs, Thanksgiving
11/27/19 W15 Projects due
11/30 3PM Last checkup opphy
12/3 RRR week porn
12/14 Final Exam

Questions 8 and of CP4 are fair game

- CP & PF both access SDRAM "directly"
  - through processor
  - Known as DMA - direct memory access
  - reality is that it isn't "direct" - need a
    DMA controller (Reg. Controller) to mediate

Why DMA?

---

Interfaces to I/O

\[
\text{polling, for interrupts, DMA}
\]

Ports

\[
\text{ memory map
  DMA}
\]

sw0 UART_TX, #4
sw1, sw0 # map to HW

sw2, sw1, sw0 ports, as x86

sw3 UART_TX

sw4 Frame buffer, memory mapped
  actually in RAM

CS150
12-FA
W13-L1
Pixel fetcher: input frame address (in)

GP: cmd list (in)
frame address (out)

SW: cmd list (out)

\[ SW \rightarrow GP \rightarrow PF \]

write ends, clear, render in same frame

2 separate, more time, more latency
Often peripherals use a combination:
- Memory mapped control registers
- DMA for data
- interrupts for notifications
- polling to figure out what happened

Data is generally going to/from MEM.
MP has an ISR latency $T_{ISR}$
Peripheral has some storage $S$

If $G/T_{ISR} > S$ lose data.
$C/T_{ISR} > S$ lose output signal?

Need $S/T_{ISR, max} > G$ (or $C$)

Example

Peripheral generator $G_{[B/s]}$ Storage

Peripheral consumer $C_{[B/s]}$ Storage

So make $S$ bigger or $T_{ISR}$ smaller.

$G = \approx 10$ KB/s WANT

$S = 1$ B need $T_{ISR, max} < G$ = $\frac{1B}{10^4 B/s} = 10^{-4}$ s

not a problem for project.

For PC? no way.

Video $G = 1.5$ MB/s
Would $S = 1$ B work?
(FIFO)

So add more S inside pipeline

\[ \text{IRQ} \]

\[ \text{G} \rightarrow \text{S} \rightarrow \mu \text{P} \]

\[ \text{why do you generate IRQ?} \]

1st byte? could be inefficient
1st byte? back to s=1 case
\[ S/2 ? \]

all make sense in different contexts

EX

ADC, DAC
even 2nd order nts need accurate sample interval

error in time is equivalent to
error in value

\[ \text{need } (4t_{\text{error}}) \leq (\text{max step size}) < \text{LSB} \]

\[ \left[ \frac{\text{LSB}}{3} \right] \]

EX, cont

MMIO registers:

\[ \text{top, m16, } \text{rate} \]

#sample
interp? configure

DMA for samples
GP & IF do DMA
DMA controller has many ports, each w/ a ready/valid interface, data, & addr.
af_addr_din, af_din addr F1F0 315
af_end_din 36

Writes
31
af_addr_din
18
wdf_din
16
wdf_mask_din

need to do twice to
put 256 bits
{← af_full
← wdf_full
→ wdf_wren
→ af_wren
valid
ready (low)

GP connects
0x0D, 000000 STOP
0x01 RR66BB FILL
0x02 RR66BB LINE
P+1 top 2 bytes X, Ylen Y
P+2 for readability

Reads
← af_end_din
← rdf_din
← rdf_readen
← rdf_data_valid
← af_full
← af_wren
twice to get
256 B