Video

SVGA 800x600 @ 75Hz

480,000 pixels/frame

36 Mpix/sec.

525 pixel clock = 49.5 MHz
16.76 µs

Visible 800 Front panel

Sync 80 160

Why? Philo T. Farnsworth!

Frame video

600 Visible

1 Front panel

16 Back panel

625 Total

(625)(1056)(75) = 49.5 MHz

pixel/line cm/s

\[ t_{\text{pixel}} = \frac{1}{47.5 \text{MHz}} = 20 \mu s \]

line = 1056 + t_{\text{pixel}} = 21.33 \mu s
Pixel fill (emulating "clear screen")

\[\text{for } (x = 0; x < 799; x++)\]
\[\text{for } (y = 0; y < 600; y++)\]
\[\text{if } \text{frame}[x][y] = \text{color} \{\]
\[\text{frame}[x][y] = \text{color}\}
\[\text{inc inner loop}\]

Line drawing:
- color \((x_0, y_0) (x_1, y_1)\)
- Bresenham is fast, no multiply or divide
- Integer only
- for shallow slopes \(x_0 < x_1 \text{ and } y_0 < y_1\)
  \[
  \Delta x = x_1 - x_0; \quad \Delta y = y_1 - y_0
  \]
  \[
  \text{error} = \Delta x / 2; \quad \text{shift, red divide}
  \]
  \[
  y = y_0;
  \]
  \[
  \text{for } (x = x_0; x < x_1; x++)\]
  \[
  \text{plot}(x, y);
  \]
  \[
  \text{error} = \text{error} - \Delta y;
  \]
  \[
  \text{if } (\text{error} < 0)\]
  \[
  y++;\]
  \[
  \text{error} + = \Delta x \times \frac{3}{3}
  \]

int frame[2][1024][1024];

for \((y = 0; y < 600; y++)\)
for \((x = 0; x < 800; x++)\)
frame[dx][y][x] = color;

better LD:
- \(\text{sw} \#a_0, 0(\#t0)\)
- \(\text{sw} \#a_0, 4(\#t0)\)
- \(\text{sw} \#a_0, 8(\#t0)\)
- \(\text{sw} \#a_0, \#l0\)
- \(\text{ble} \#t0, \#t2, \text{letter l0}\)
- \(\text{addi} \#t0, \#t0, 64\)

Other things to draw:
- Characters
- Boxes, filled boxes
- Triangles, filled trapezoids, shaded triangles
Dram Intel 1101, 1103

1970, 1K5, $10, 500ns, 3x3mm^2

Today 4G6? ~ 50ns? ~ 8x8mm^2

Early DRAM was asynchronous (no CLK)

Shared row/col address lines and "strobe" signals to latch

RAS = row addr. strobe
CAS = col. addr. strobe

Generally active low \( \overline{RAS} \text{ or } \overline{CAS} \)

destructive read, refresh
must read/write every \( 2^m \) every 64ms (32ms adaptive)
to read values on same row:
- present row addr.
- $RAS^+$
- wait
  - $WE = 0$
  - present col addr
- $CAS^-$
- present new col addr.
- $CL$
- $CAS$ latency
- $RCD$
- Row to column

To read on different row:
- $A = Row 1$
- $RAS^+$
- $wait$
- $A = COL 1$
- $CAS^-$
- $wait$
- $RAS^-$
- Write back
- $CAS^-$
- Precharge
- $A = Row 2$
- $RAS^-$

Modifications:
- Multiple output bits

Multiple banks:
- Since $t_{RCD}$ can be long
- $t_{CL}$
- Have separate row regs for separate parts of chip

$2^m$ lines total in groups of $K$