Announcements

• Homework #2 due today
  - Drop box in 240 Cory

• Homework #3 out later tonight
  - Due next Thurs.

• Next Tues. (9-20) lecture will be taped ahead
  - 12:30-2pm, 306 Soda
  - Please do attend if you can
Overview of Physical Implementations

The stuff out of which we make systems.

- **Integrated Circuits (ICs)**
  - Combinational logic circuits, memory elements, analog interfaces.
- **Printed Circuits (PC) boards**
  - substrate for ICs and interconnection, distribution of CLK, Vdd, and GND signals, heat dissipation.
- **Power Supplies**
  - Converts line AC voltage to regulated DC low voltage levels.
- **Chassis (rack, card case, ...)**
  - holds boards, power supply, fans, provides physical interface to user or other systems.
- **Connectors and Cables.**

### Integrated Circuits

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 100 - 1000M transistors
- (25 - 250M "logic gates")
- 3 - 10 conductive layers
- 2011 - feature size ~ 28nm = 0.028 x 10^-6 m
- "CMOS" most common - complementary metal oxide semiconductor

**Chip in Package**

- Package provides:
  - spreading of chip-level signal paths to board-level
  - heat dissipation.
- Ceramic or plastic with gold wires.
Chip-level Function Implementation Alternatives

Full-custom: All circuits/transistor layouts optimized for application.

Standard-cell: Arrays of small function blocks (gates, FFs) automatically placed and routed.

Gate-array: Partially prefabricated wafers customized with metal layers.

FPGA: Prefabricated chips customized with switches and wires.

Microprocessor: Instruction set interpreter customized through software.

Domain Specific Processor: (DSP, NP, GPU).

Reminder: FPGAs are interesting because of low design cost.
How To Think About CMOS Transistors

- CMOS transistors are just switches!

**NMOS:** on when “$V_G$” is high

- $V_{GS} > V_T$
  - $V_{GS} < V_T$
  - $V_{GS} < |V_T|$
  - $V_{GS} > |V_T|$

**PMOS:** on when “$V_G$” is low

- $V_{SG} < |V_T|$
- $V_{SG} > |V_T|$

Transistor-Level Logic Circuits

**Inverter (NOT gate):**

**NAND gate:**
CMOS Logic Gates in General

- Pull-up network conducts under conditions to generate a logic 1 output
- Pull-down network conducts for logic 0 output

CMOS Transistors as Switches Revisited

- NMOS only to pass logic zero (pull-down)
- PMOS only to pass logic one (pull-up)

- Show why by counter-example: NMOS driving logic one

- Note: “weird” analog and some digital designs will occasionally break these rules...
Switch Logic Connections

- Switches in series: AND
- Switches in parallel: OR

CMOS Logic Gates in General

Implications:

1. Pull-up and pull-down networks are complementary
2. Pull-up and pull-down networks are topological duals (DeMorgan)

Pull-up and pull-down networks should never both be on - else, short circuit!
CMOS Transistors as Switches Revisited (2)

- Can build an “ideal” switch that passes both 0 and 1
- “Transmission gate”
  - NMOS passes logic 0, PMOS passes logic 1

- Note: eventually need to combine with a “normal” CMOS logic gate to get restoration (buffering)
  - Transmission gate by itself is bi-directional

Transmission Gate MUX

2-to-multiplexor:  
\[ C = s_a + s'b \]

Switches simplify the implementation:

Compare the cost to logic gate implementation.
**4-to-1 Transmission-Gate Mux**

- The series connection of pass-transistors in each branch effectively forms the AND of s1 and s0 (or their complement).
- Compare cost to logic gate implementation

**Alternative 4-to-1 Multiplexor**

- This version has less delay from in to out.
- In both versions, care must be taken to avoid turning on multiple paths simultaneously (shorting together the inputs).
Tri-State Buffers

Tri-state Buffer:

```
<table>
<thead>
<tr>
<th>CE</th>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
```

“high impedance” (output disconnected)

Variations:

- Inverting buffer
- Inverted enable

Transmission gate useful in implementation

Tri-State Buffer Uses
Latches and Flip-Flops