UNIVERSITY OF CALIFORNIA, BERKELEY
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Department of Electrical Engineering and Computer Sciences

Elad Alon **Homework #4** **EECS150**

Due Thursday, September 29, 5pm, box in 240 Cory

1. This is a two part problem; please use the modifications you make to the processor in a) to do b).

   a) DDCA 7.4, but add support for both *lwinc* and *swinc*:
   swinc ***$rt,*** ***imm($rs)*:**
   sw *$rt,* *imm($rs)*
   addi *$rs,* *$rs,* *4*

   b) Using Table 7.6 (pg. 381) and given that every read or write port you add to the register file increases register file read delay by 20ps, what is the cycle time of the modified processor?

Table 7.6 Delays of circuit elements

Element	Parameter	Delay (ps)
register clk-to-Q	t_{pcq}	30
register setup	t_{setup}	20
multiplexer	t_{mux}	25
ALU	t_{ALU}	200
memory read	t_{mem}	250
register file read	t_{RFread}	150
register file setup	$t_{RFsetup}$	20

2. DDCA 7.10 using (a), (b), and (c) from 7.3

3. As in DDCA 7.24: Which registers are being written, and which are being read on the eighth cycle of the following set of instructions? (Optional: can you figure out what is in the registers $s0-$s4 by the end?)
   addi $s0, $0, 115
   subi $s1, $s0, 16
   addi $t0, $0, 1
   sll $t1, $t0, 5
   srl $t2, $t1, 1
   add $t3, $t1, $t0
   srl $t4, $t2, 2
   add $s2, $t3, $t0
   add $s3, $s2, $t4
   sub $s4, $s2, $t0

4. DDCA 7.26

5. DDCA 7.30