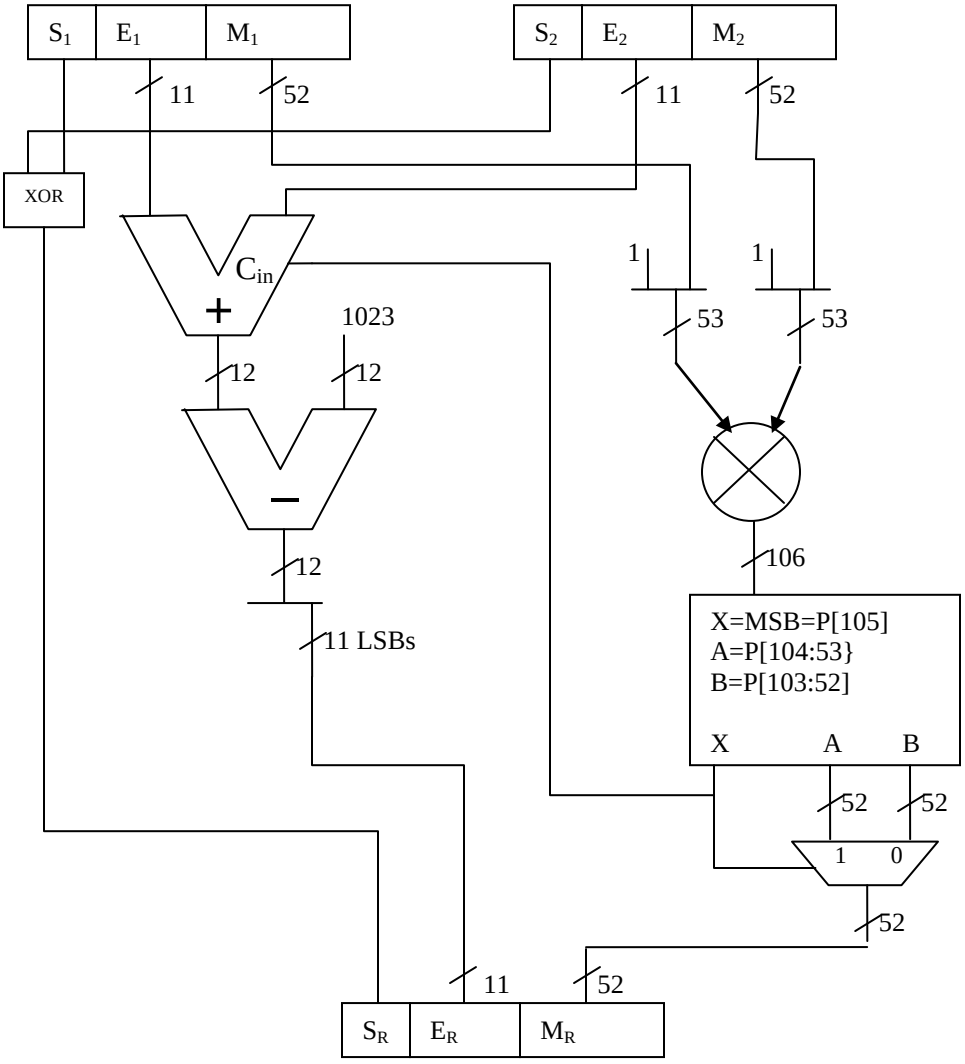
HW Quiz 8
EECS150, Fall 2010 NAME_____ SID_____

1. Design a **single-cycle** double-precision (64-bit) floating point multiplier. You may use shifters, adders, fixed-point multipliers, etc. in your design. If you need special combinational logic, describe its function (don't implement with gates unless that's easier). Clearly show the data inputs and outputs, bit widths of all lines, etc. Show clearly how the sign, mantissa, and exponent of the Result are obtained. Don't worry about special cases (underflow, overflow, NaN inputs, denormalized inputs, etc.) – just design for the general case of normal inputs that should generate a normal output.



$(1.M_1)(1.M_2) = XY.R$ and XY must be 01, 10, or 11. If X=1, then increment exponent (using C_{in}), and M_R is the first 52 bits of Y R. If X=0, then M_R is the first 52 bits of R.

The exponents are stored biased by 1023. Adding two exponents means we have an extra bias, so need to subtract one of them.