Homework 4
Fall 2010
CS150

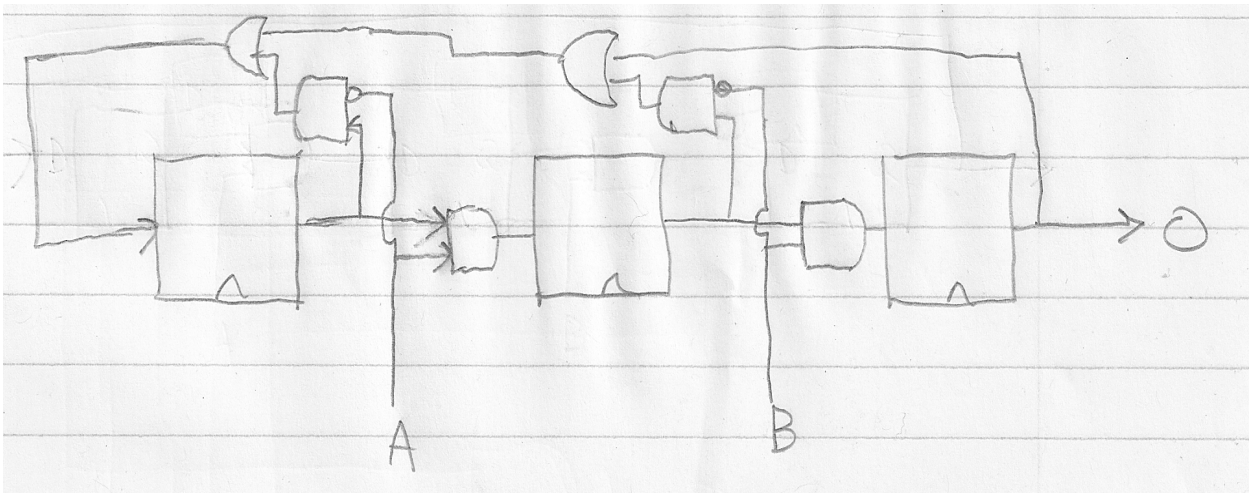
3.15)

(a) Is not a synchronous sequential circuit because there is no register.
(b) Is not a synchronous sequential circuit because there is a combinational loop.
(c) Is a synchronous sequential circuit because the feedback loop is on the other side of a register.
(d) Is also a synchronous sequential circuit because the feedback loop is on the other side of the register.

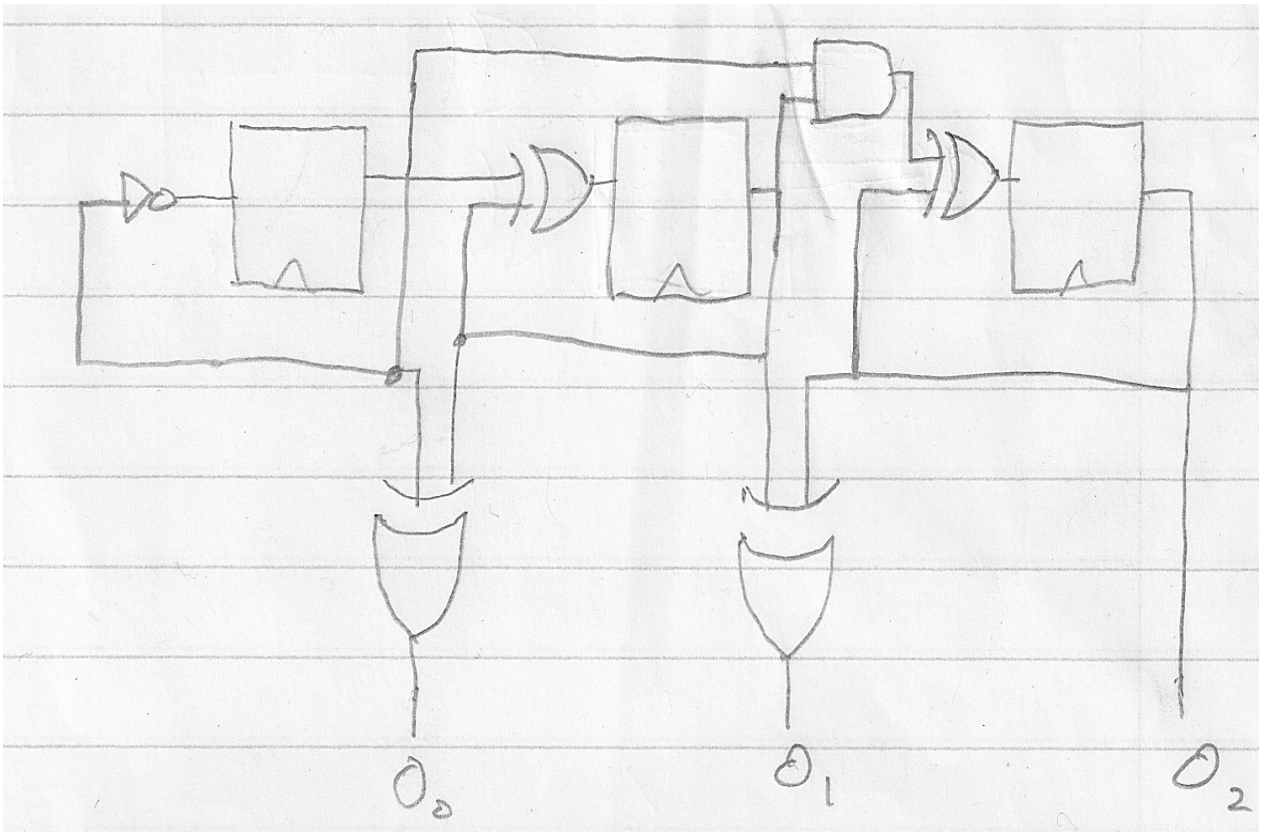
3.19)

This FSM has two inputs A and B, and an output Q. Q_n is high when A_{n-2} is high and B_{n-1} is high, otherwise it is zero.

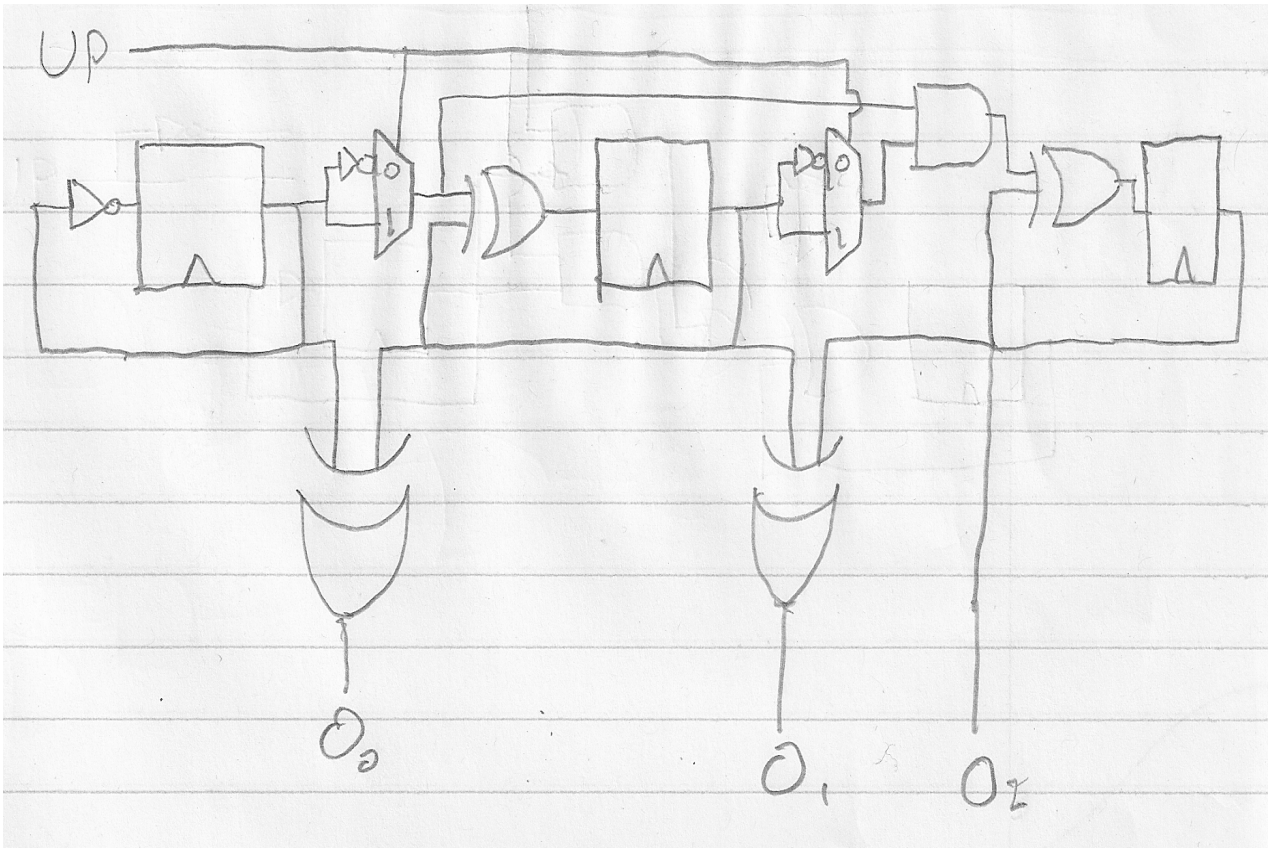
CS	NS	A	B	O
S0	S0	0	X	0
S0	S1	1	X	0
S1	S0	X	0	0
S1	S2	X	1	0
S2	S0	X	X	1



3.24)

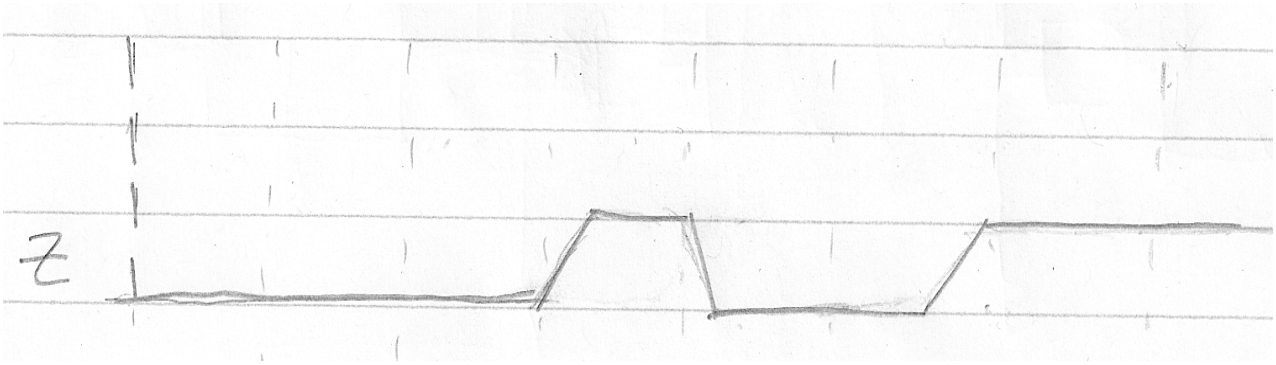


3.25)



3.26)

(a)

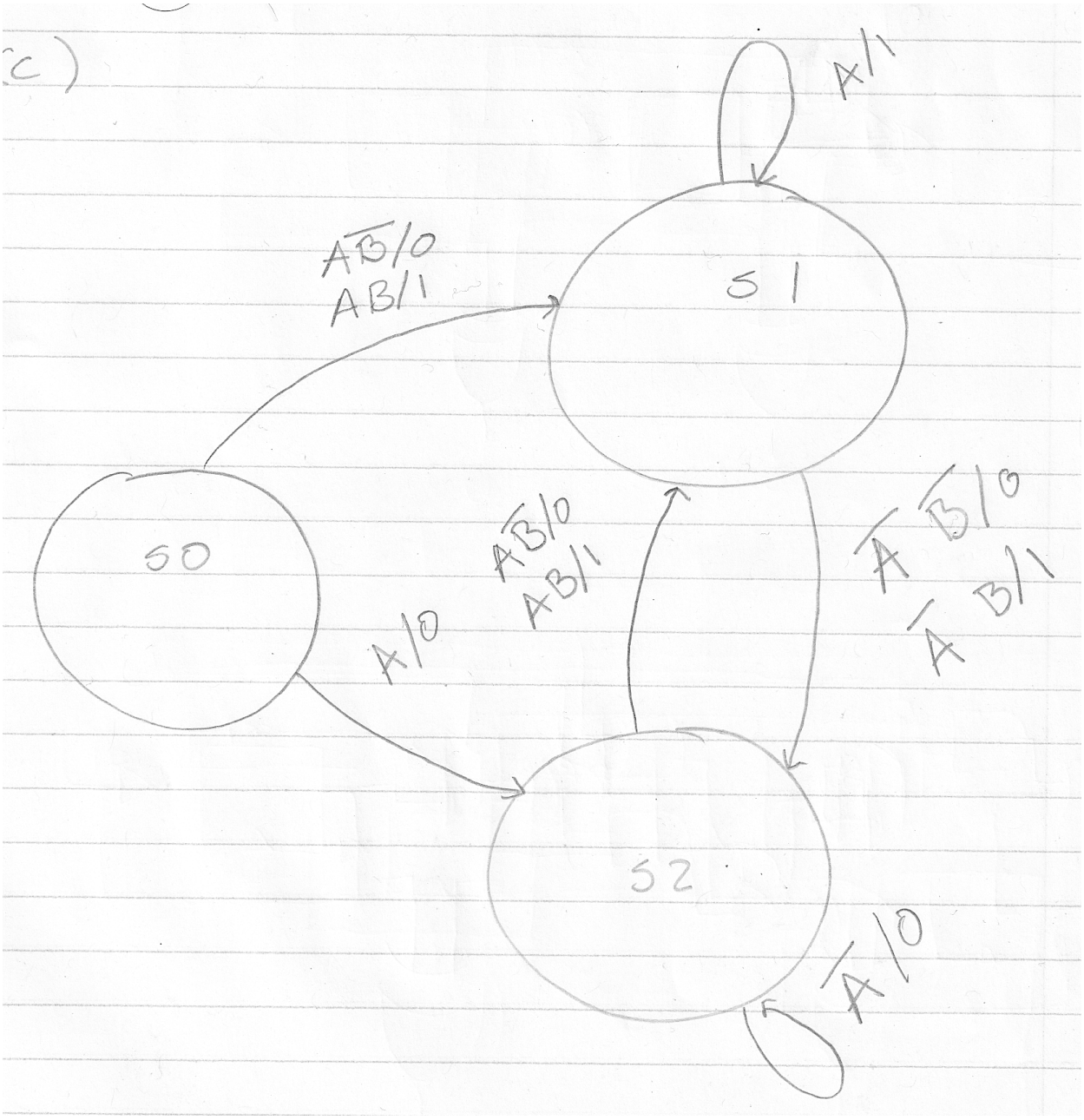


(b) Mealey

(c)

CS	NS	A	B	Z
S0	S1	1	0	0
S0	S1	1	1	1
S0	S2	0	X	0
S1	S2	0	0	0

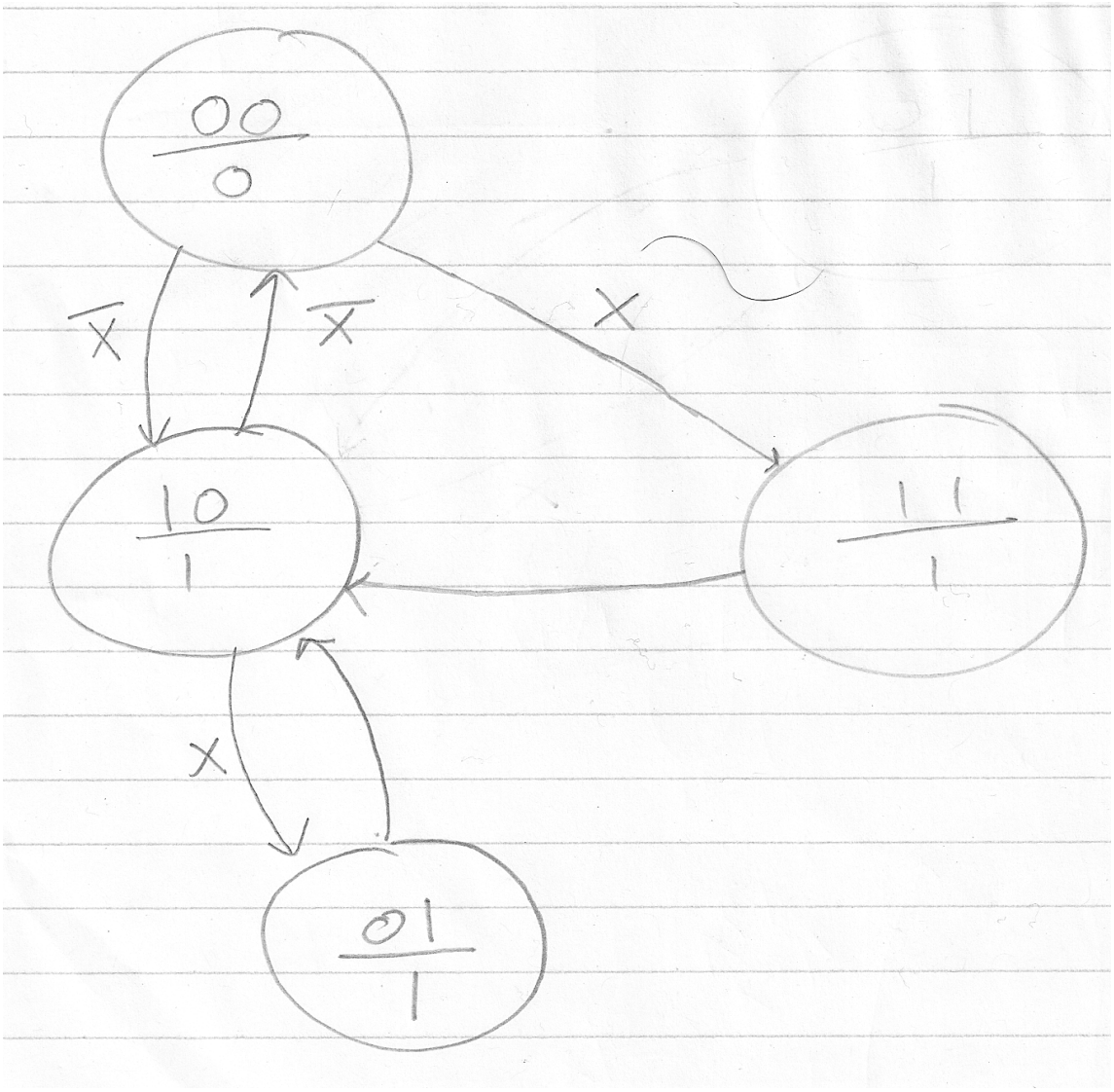
S1	S2	0	1	1
S1	S1	1	0	1
S1	S1	1	1	1
S2	S2	0	0	0
S2	S2	0	1	0
S2	S1	1	0	0
S2	S1	1	1	1



3.28)

CS	NS	X	Q

00	10	0	0
00	11	1	0
01	10	X	1
10	00	0	1
10	01	1	1
11	10	X	1



3.30)

(a) ClockPeriod = clock-to-Q_max + 3 * xor_delay + setup
= 70ps + 3 * 100ps + 60ps
= 430ps
OperatingFrequency = 1 / 430ps
= 2.33GHz

(b) 1 / 2 GHz = 500ps
Tolerable skew = 500ps - 430ps = 70ps

(c) The path through the bottom XOR gate is the

one we need to worry about. Since the contamination delay of the XOR gate is 55ps and the clock-to-Q minimum delay of the flip flop is 50ps. Therefore clock skew of up to 55ps + 50ps - 20ps = 85ps is tolerable.

(d) Here circuit is a balanced tree. It has a period of 70ps + 2 * 100ps + 60ps = 330ps, a frequency of 3.03GHz. As for hold time violations, this new circuit adds an XOR in the shortest path, therefor the maximum tolerable skew is now, 55ps + 2 * 50ps - 20ps = 135ps.

3.31)

(a) ClockPeriod = clock-to-Q prop + AB2Co + Ci2S + setup
= 35ps + 25ps + 3ps + 30ps
= 110ps
OperatingFrequency = 1 / 110ps = 9.09GHz

(b) ClockPeriod = 1 / (8GHz) = 125ps
TolerableSkew = 125ps - 110ps = 15ps

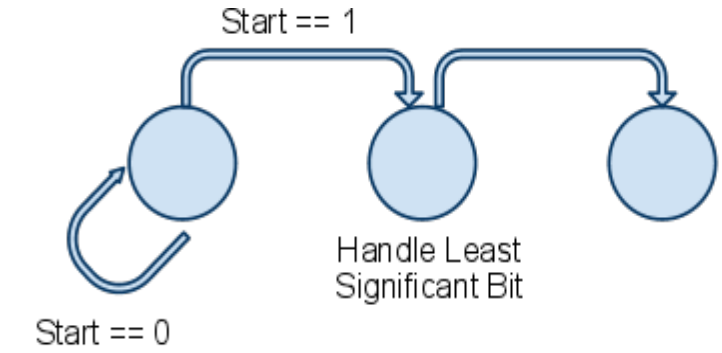
(c) Since the contamination delay of the Adder from Cin to either output is 15ps and the hold time is 10ps, there is tolerable skew of 5ps.

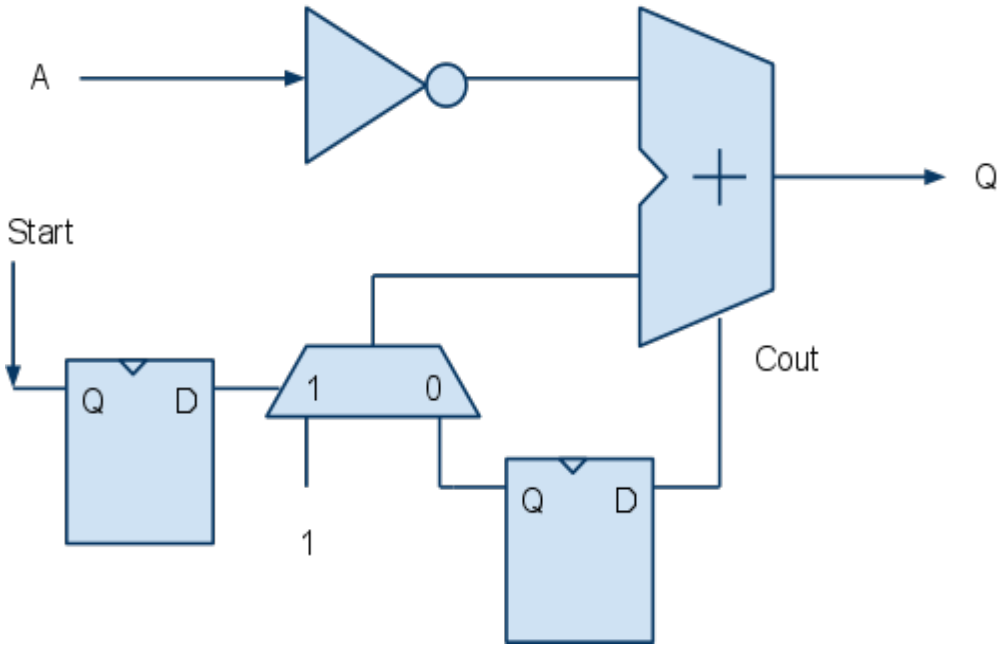
3.32)

(a) ClockPeriod >= clock2Q + N * CLB prop + setup
1 / 40MHz >= .72ns + N * .61ns + .53ns
25ns >= 1.25ns + N * .61ns
N <= 38

(b) TolerableSkew = clock2Q cont + CLB cont
= .50ns + .30ns
= .80ns

Interview Question 3.2


Start == 1
Handle Least
Significant Bit
Start == 0


A
Q
Start
Cout
Q
D
1
0
1
Q
D