EECS150: Homework 3, Boolean Logic, Flip Flops, Counters and Verilog

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1 Time Table

ASSIGNED	Thursday, September 4^{th}
DUE	Friday, September 12^{th}

1. Given the BCD−to−7−seg functions given in CLD2 Figure 2.25:
   (a) Write C1 in minterm and maxterm form, and draw the logic gates to implement the canonical two level SoP and PoS forms.
   (b) Do the same for C5.
   (c) Does one implementation take fewer gates in either case? Why?
2. Figure 6.25 in CLD2 has one labeling error. Figure 6.26 has 3. Find them (and fix them in your book!).
3. CLD2 problems:
   (a) 6.12
   (b) 6.14
   (c) 7.1
   (d) 7.2
4. Is it possible to write two different Boolean expressions (both in minimized SoP form) which have the same truth table? Is it possible to write two different truth tables which have the same Boolean expression? If you answer yes to either question, give an example. If no, explain why.
5. Go to digikey.com and find one of the cheapest dual J−K flip flop that you can (don't kill yourself trying to find the absolute cheapest one − there are something like 6,000 different flip flops to choose from. It should be way less than $1.00 dollar, that's what matters)
   (a) What is the cost per flip flop?
   (b) The Xilinx XCV2000E on your Calinx board has over 43,000 flip flops. How much would just the flip flops cost if you needed to build the XCV2000E functionality using dual J−K flip flops? Look up the cost of this part. You are looking for the xcv2000e part in a fg680 package, commercial (c) temperature standard, and speed grade -6.
   (c) What's the cheapest Xilinx FPGA (not CPLD!) that you can find on digikey? How many flip flops does it have? (Hint: Digikey does not allow you to sort by price easily. Find the cheapest device in a few of the Xilinx's device families, and compare those. Older devices are not necesarily cheaper than new ones.)

(d) If you need a really cheap fix to a digital problem on a board that you're designing, for very simple solutions with just a few flip flops, discrete dual J−K packages will be the cheapest solution. What's the crossover point where a xilinx part will be cheaper?

6. Erroneous Verilog. Each of the following reference a code fragment and (where appropriate) indicate what the user intended to construct in Verilog. Find and explain the bugs.

   (a) Program 1. The user wanted to create a shift−register.

   (b) Program 2.

   (c) Program 3.

Program 1 Problem 6a

```
wire Input;
reg RegisterB, RegisterC, RegisterD;

always @(posedge Clock) begin
    RegisterB = Input;
    RegisterC = RegisterB;
    RegisterD = RegisterC;
end
```

Program 2 Problem 6b

```
wire Input, B;
reg RegisterB, RegisterC, RegisterD;

assign A = Input | RegisterC;
assign RegisterB = Input & RegisterC;

always@( * ) begin
    B = Input | RegisterC;
end
```

Program 3 Problem 6c

```
wire Condition, Input;
reg A, B, C;

always @( * ) begin
    A = 1'b0;
    if (Condition) begin
        B = Input;
        C = Input;
    end
    else begin
        B = Input;
    end
end
```