University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

SOLUTIONS

EECS 150 K. Pister
Fall 2006

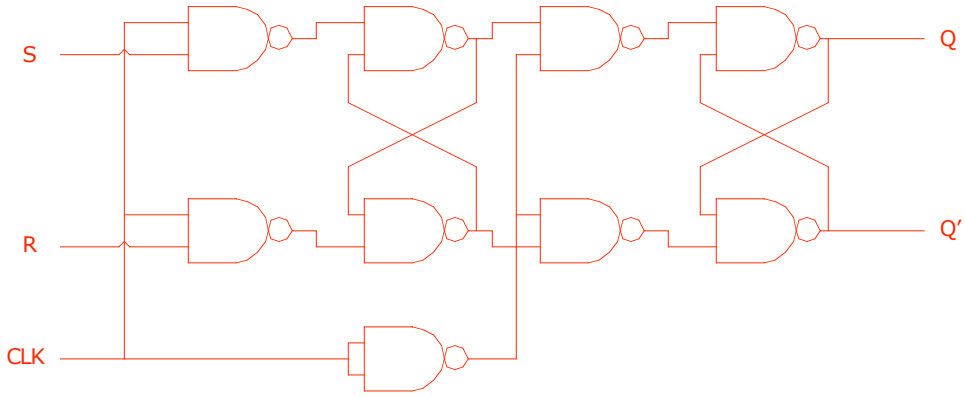
Problem Set #3

For this assignment, assume that the propagation delay of NAND and NOR gates is 100ps, and inverters are 30ps.

1. [graded, quiz material] In figure 6.13, what is the minimum time that *enable* must be asserted in order to guarantee that the input values on S' and R' will have their desired effect on the output of the latch?

   We need minimum $2*D_{NOR} = 200$ ps

2. [graded, quiz material] Re-draw the master-slave flip flop in figure 6.18 using only NAND gates and one inverter.



   a. What is the propagation delay from an input change to the output of the master flip flop (assuming the clock is high)?

      200ps (for the shorter time) or 300ps (for the longer time)

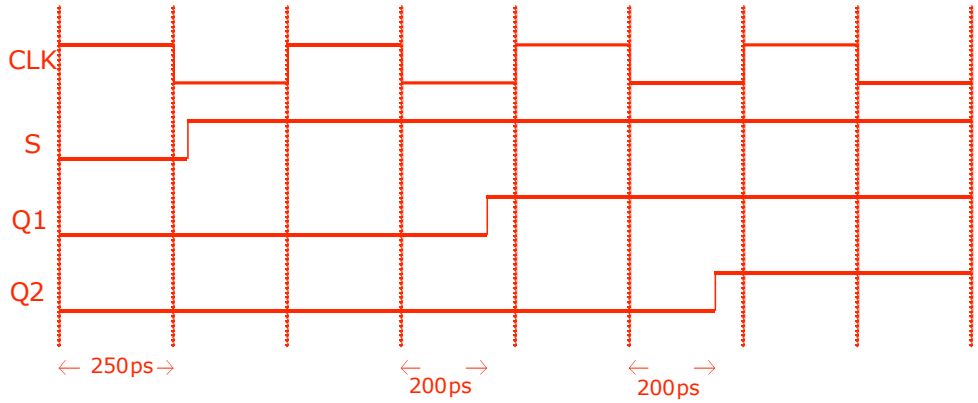
   b. What are the setup and hold times for this flip flop?

      Setup time is officially 200ps, but any solution < 250ps with good justification is valid. Hold time is 0ps.

3. [graded] Same question, but just draw the clock, set input, and Q_1 and Q_2. Label your time axis carefully!

   First, not that a 2 GHz clock gives us a period of 500ps and a duty cycle of 250ps, so we will base our timing diagram on this:

   a. Draw a timing diagram showing the outputs of all of the NAND gates (there should be 16 of them) assuming a 2GHz clock. Show as many cycles as you need until all of the outputs remain constant.



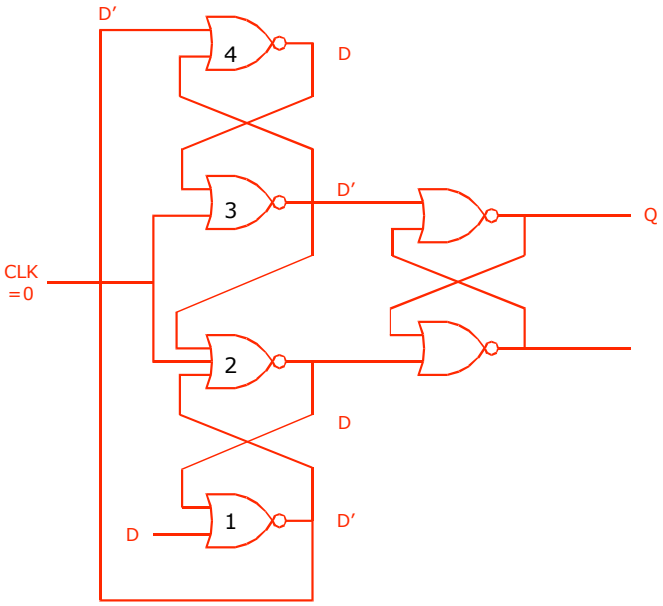
b. What is the fastest clock that could be used with this state and input combination.

Recall that $t_{cycle} >= t_{prop} + t_{setup} + t_{cl}$. Considering that there is no combinational logic (outside of that used to generate the flip flops) we have $t_{cycle} >= t_{prop} + t_{setup}$. From #2 above, we know that that $t_{prop,max}$ = 300ps and t_{setup}=200ps, giving us a t_{cycle} of 500ps. This works out to be a 2GHz clock.

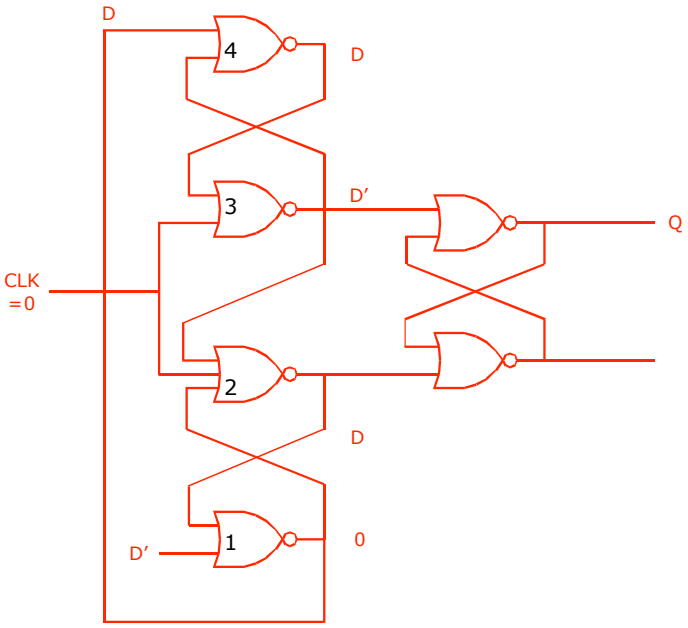
c. What would happen if both set and reset go high and remain high?

If S and R are both held high, then the master stage of the first flip flop will have unknown outputs when the clock is high; when it goes low, it will stabilize to either Q or Q'. The final output of the first flip flop will come sometime after the falling edge and will get fed to the second flip flop, which will always hold the previous value of the first.

4. [Graded] Figures 6.25 and 6.26 contain a total of 4 errors in the logical values present at the nodes. Find them and fix them in your book! Redraw the correct figures here.



CLK	1 ->	0 ->	0 ->	0 ->	0
1	D' ->	D' ->	D' ->	D' ->	D'
2	0 ->	0 ->	D ->	D ->	D
3	0 ->	0 ->	D' ->	D' ->	D'
4	D ->	D ->	D ->	D ->	D



CLK	1 ->	0 ->	0 ->	0 ->	0
1	0 ->	D' ->	0 ->	0 ->	0
2	0 ->	0 ->	D ->	D ->	D
3	0 ->	0 ->	D' ->	D' ->	D'
4	D ->	D ->	D ->	D ->	D

5. [Quiz material, graded] What are the setup and hold times for the flip flop in figure 6.26?

   $t_{setup} = t_{hold} = 2*t_{NOR} = 200ps$