

1. Note the pattern:

square #	# grains	... in binary	bits
1	1	1	1
2	2	10	2
3	4	100	3
4	8	1000	4
⋮	⋮	⋮	⋮
k	2^{k-1}	$1\underbrace{00}_{k-1 \text{ times}}$	k

a. From the table, k

b. From the table, 2^{k-1}

c. A chess board has 64 squares so we have,

$$\sum_{k=0}^{63} 2^k = 2^{64} - 1 = \underbrace{11\dots1}_{64}_2 = 1.845 \times 10^{19} \text{ grains}$$

d. If one grain is 10 mm^3 , the total volume is
 $(1.845 \times 10^{19} \text{ grains})(10 \text{ mm}^3/\text{grain}) = (1.845 \times 10^{20} \text{ mm}^3)(10^{-9} \text{ m}^3/\text{mm}^3)$
 $= 1.845 \times 10^{11} \text{ m}^3$

Therefore, the depth of the pile would be

$$1.845 \times 10^{11} \text{ m}^3 / (.3 \text{ m})^2 = 2.05 \times 10^{12} \text{ m}$$

2a.

$$\begin{aligned} & 50\,000 \text{ gates} \\ 8192 \times 8 &= 65\,536 \text{ "gates" from RAM} \\ 65\,536 / 10 \times 8 &= 52\,428.8 \text{ "gates" from ROM} \\ \hline & 167\,964.8 \text{ total "gates" per ASIC} \end{aligned}$$

The size of an ASIC is

$$(167\,964.8 \text{ gates/ASIC})(100\,000^{-1} \text{ mm}^2/\text{gate}) = \boxed{1.680 \text{ mm}^2/\text{ASIC}}$$

b. A 200 mm wafer has a surface area of

$$\pi(100 \text{ mm})^2 = 31\,416 \text{ mm}^2$$

on which we can fit

$$(31\,416 \text{ mm}^2/\text{wafer})(1.680^{-1} \text{ ASICs/mm}^2) = 18\,700 \text{ ASICs/wafer}$$

With 90% yield, our usable ASICs/wafer is

$$(18\,700 \text{ ASICs/wafer})(.9) = 16\,830 \text{ ASICs/wafer}$$

With a 20% testing overhead, the cost of a wafer is \$1200
so the cost per ASIC is

$$(\$1200/\text{wafer})(16\,830^{-1} \text{ wafers/ASIC}) = \boxed{\$.0713/\text{wafer}}$$

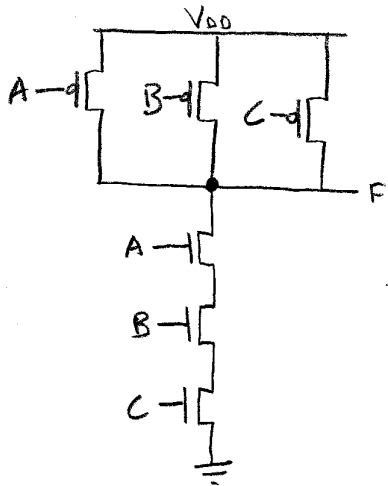
c. We save $\$10 - \$.0713 = \$9.9287$ per product, thus recouping the mask cost in

$$\$200\,000 / \$9.9287 = \boxed{20\,144 \text{ products}}$$

d. Using the same method as above,

$$\$5\,200\,000 / \$9.9287 = \boxed{523\,735 \text{ products}}$$

3. As in lecture, a 3-input NAND gate scales from the 2-input version:



Since this design requires six transistors as opposed to the standard four (of which we can fit 100 000/mm²), we assume that 66 666 can fit per mm². We can therefore fit

(66 666 gates/mm²)(31 416 mm²/wafer) = 2.094 × 10⁹ gates/wafer
of which

(2.094 × 10⁹ gates/wafer)(.9) = 1.858 × 10⁹ gates/wafer

work. It therefore costs

(\$1200/wafer)(1.858 × 10⁹ wafers/gate) = $\boxed{\$6.459 \times 10^{-7} / \text{gate}}$

You could therefore get

(6.459 × 10⁻⁷ gates/\$)(.01 \$/¢) = $\boxed{15\ 482 \text{ gates/penny}}$