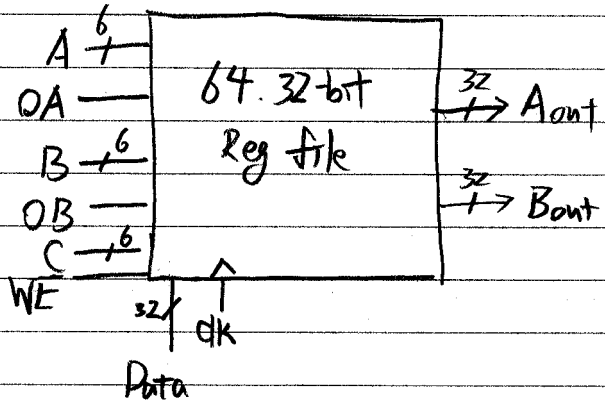
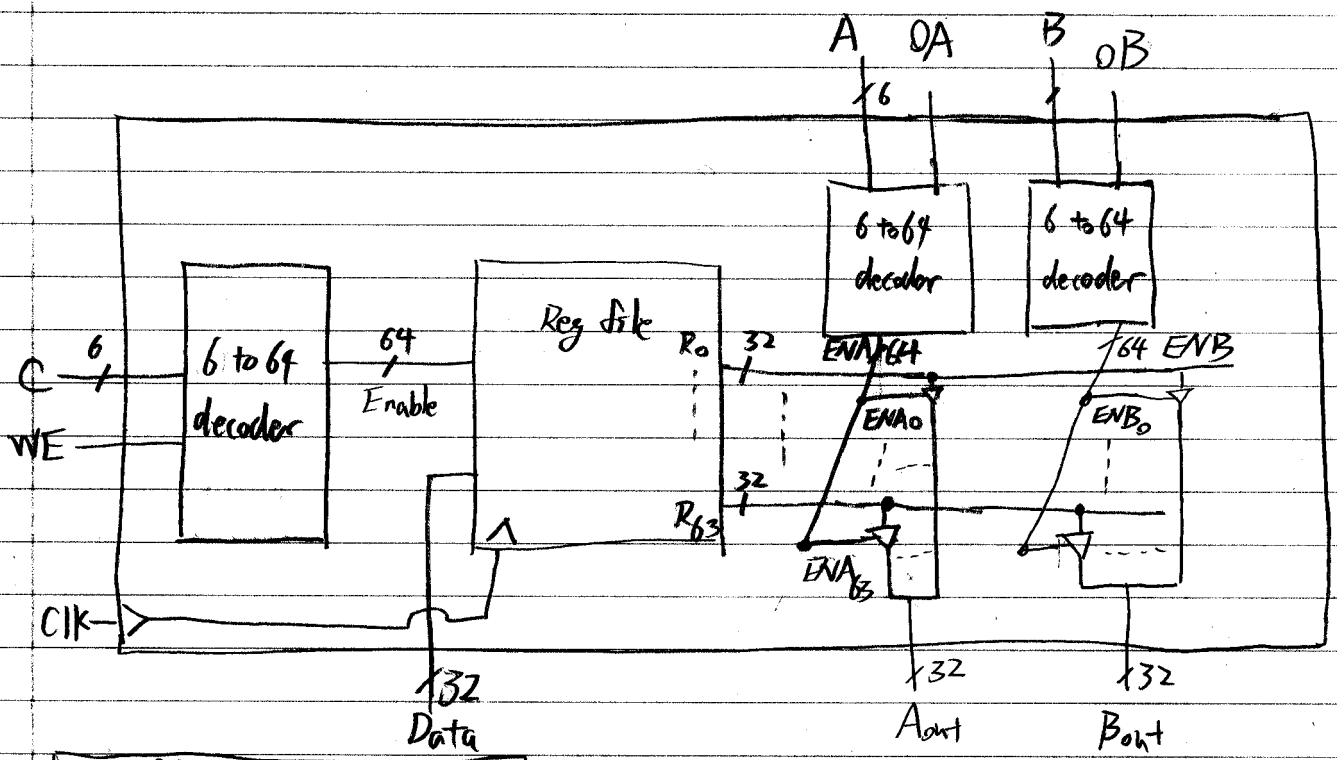
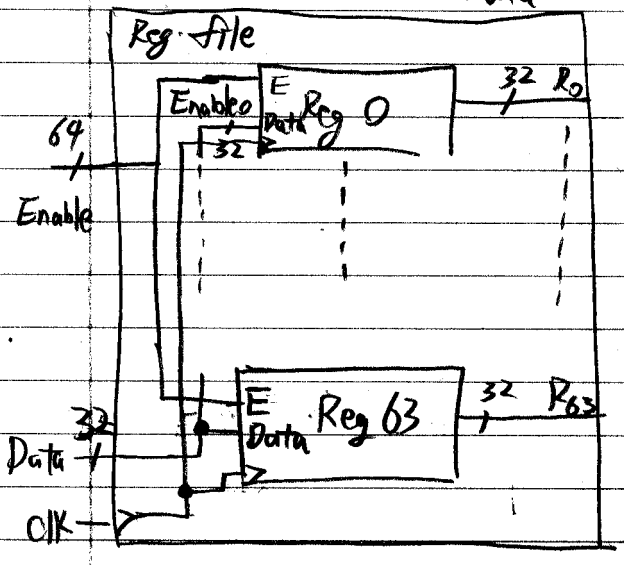
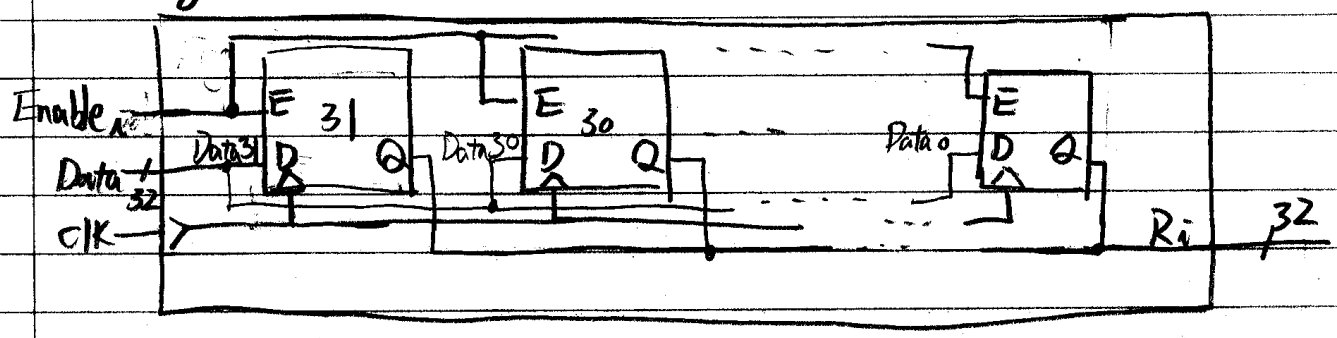
L 3-Port register



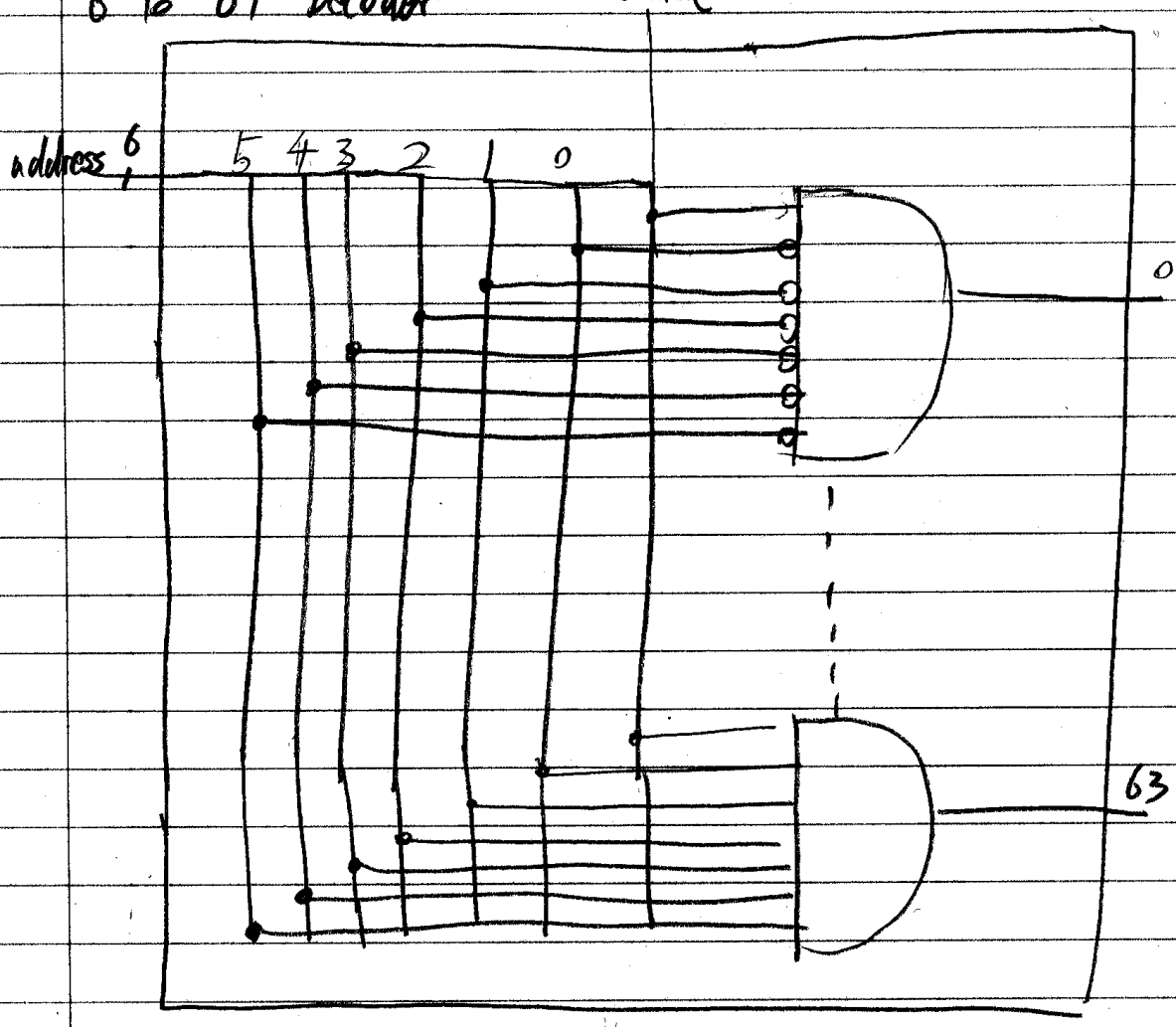




Reg i



6 to 64 Decoder



FPGA: 1 CLB = 4 slices = 8 blocks (each block has 4-input LUT and a FF)

Reg file

$64 \times 32 \times \frac{1\ CLB}{8\ FF} = 256$ CLB's

Three 6 to 64 decoders

$3 \times 64 \times \frac{1\ CLB}{4\text{-7 input AND}} = 48$ CLB's

64 × 2 tristates

$64 \times 2 \times \frac{1\ CLB}{8\text{ tristate}} = 16$ CLB's

320 CLB's

$\Rightarrow \frac{320\ CLB's}{\text{total } 9600\ CLBs} = 3.3\ \%$

CMOS:

Reg file

$64 \times 32 \times \frac{8\ gates}{\text{D-FF with Enable}} = 16384$ gates

Three 6 to 64 decoders:

$3 \times 64 \times \frac{3\ gates}{\text{7-input AND}} = 576$ gates

64 × 2 tristate

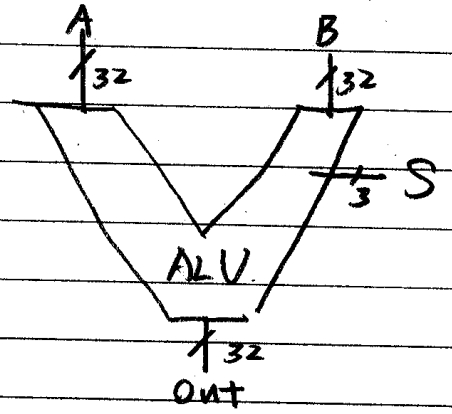
$64 \times 2 = 128$ gates

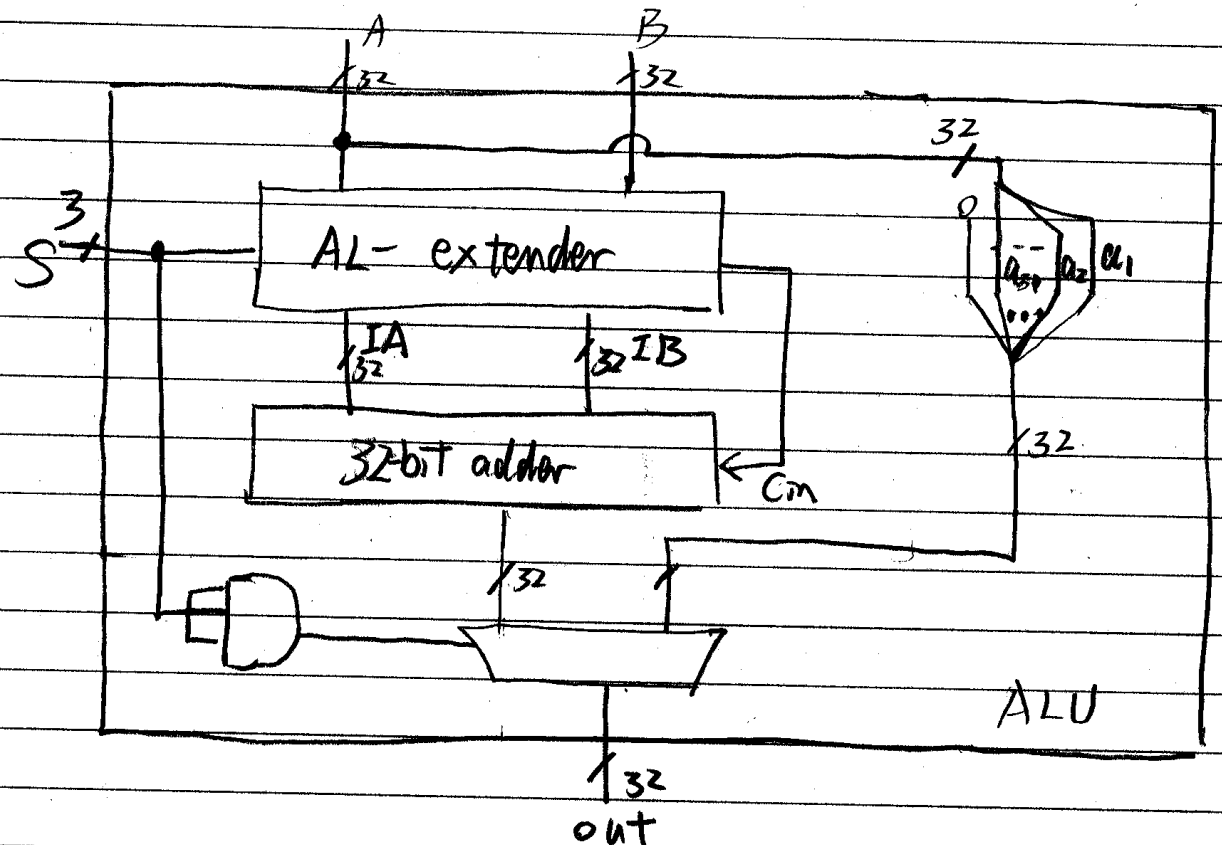
17088 gates

$\Rightarrow \frac{17088}{10^6} = 0.017\ mm^2$

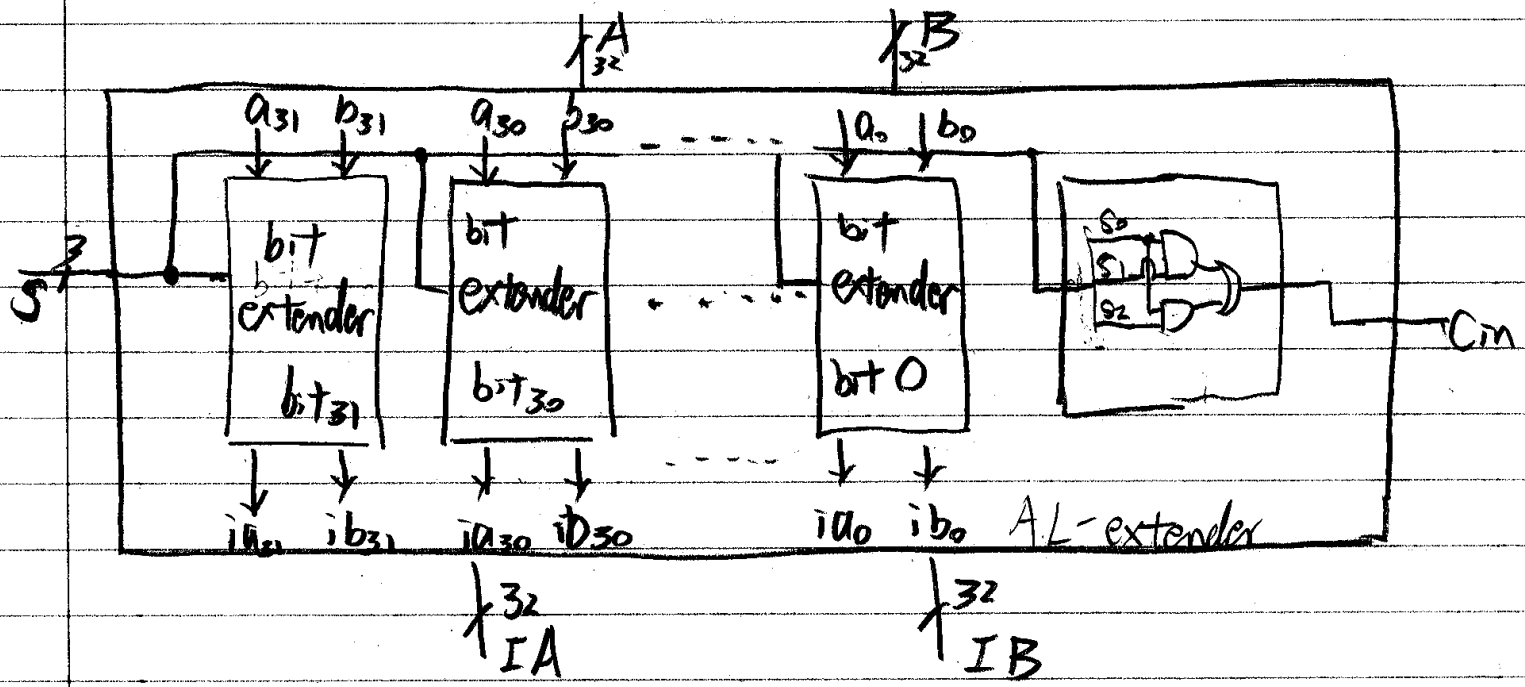
2. 32-bit ALU

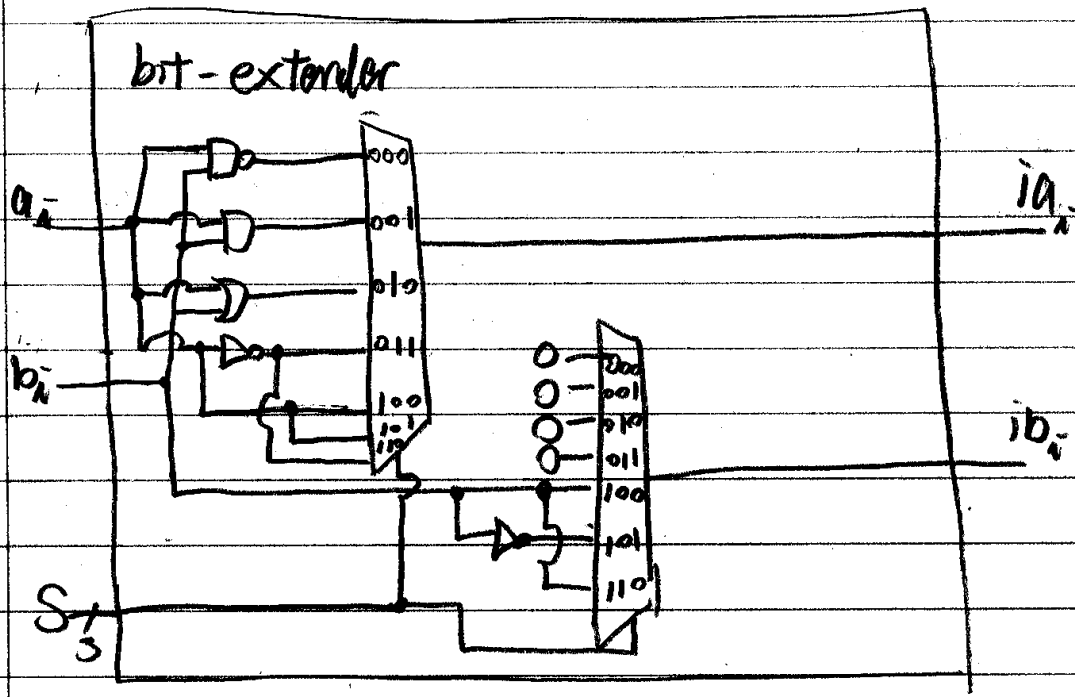
Control S_0	S_1	S_2	Operation	bit-operation	C_{in}
0	0	0	A NAND B	$ia = \overline{ab}$ $b=0$	0
0	0	1	A AND B	$ia = ab$ $b=0$	0
0	1	0	A OR B	$ia = a+b$ $b=0$	0
0	1	1	Not A	$ia = \overline{a}$ $b=0$	0
1	0	0	A + B	$ia = a$ $ib = b$	0
1	0	1	A - B	$ia = a$ $ib = \overline{b}$	1
1	1	0	B - A	$ia = \overline{a}$ $ib = b$	1
1	1	1	A/2	separate operation	X



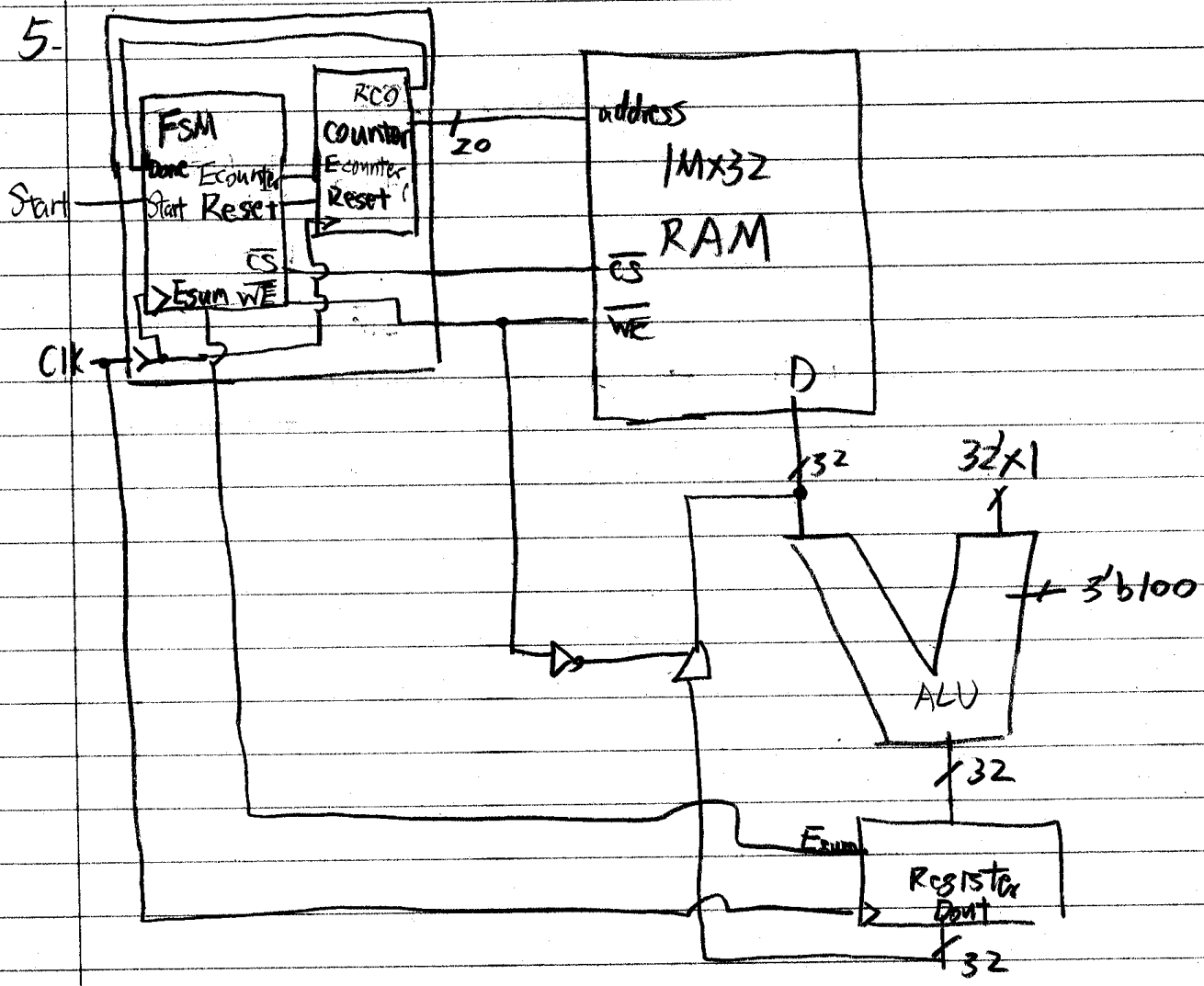


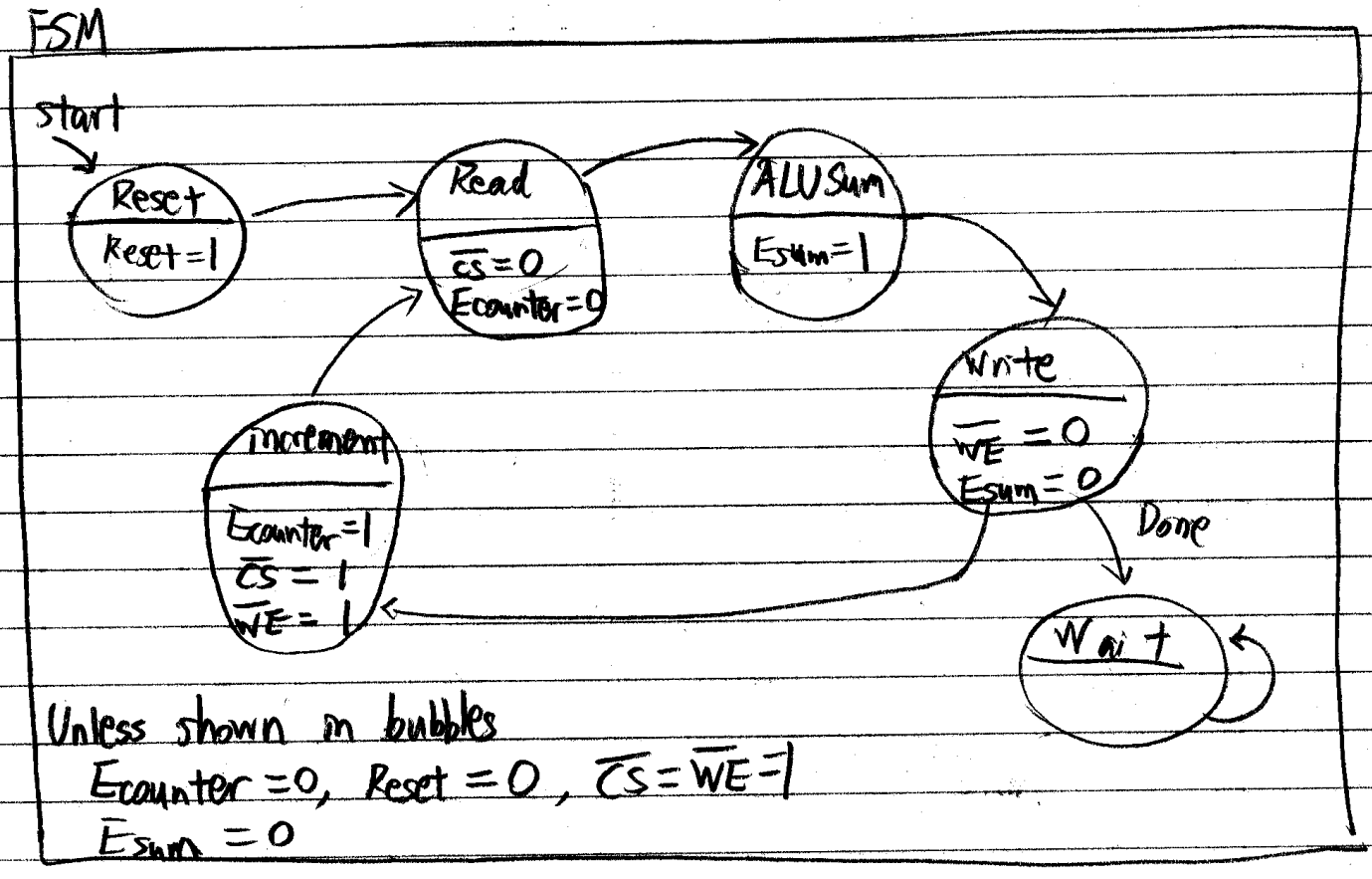
Please refer to textbook for 32-bit adder





5-





Unless shown in bubbles
Ecounter=0, Reset=0, $\overline{CS}=\overline{WE}=1$
Esum=0