

EECS150 - Digital Design
Lab Lecture – Project Grading

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Checkpoints

- 1. Network Test: [5 points]** (1 week, check-off by week of 10/21)
TA solution posted 10/25
- 2. Video Test: [5 points]** (1 week, check-off by week of 10/28)
TA solution posted 11/1
- 3. SDRAM Test: [5 points]** (1 week, check-off by week of 11/4)
Write and read data patterns to SDRAM.
TA solution posted 11/8
- 4. Frame buffer: [15 points]** (1 week, check-off by week of 11/11)
Display video from from SDRAM based frame buffer. Use buttons to control cursor position and color on screen.
No TA solution posted.
- 5. Integration, debugging, improvements.** (3 weeks, final check-off by week of 12/2) Extra credit for check-off one week early.

Project Grading

- Checkpoints contribute 30% to project grade.
- Remaining 70% based on functionality and quality.
- **Functionality (40%):** does your design perform the required function without bugs?
 - Based on in-lab final demo/checkoff.
 - We will put your design through a set of tests to try to discover conditions when it fails. (Similar tests will be made available to you earlier).
- **Quality (30%):** Based on
 - Short on-line report
 - Block diagrams of your circuits
 - Verilog descriptions
 - Your design should be easy for us to understand
 - Should try to minimize the number of FPGA LUTs, and Memory
 - You will be penalized for excessively high number of LUTs and memory and rewarded for low numbers.
- Prizes for few best designs (most compact, most features, first done,

Verilog Notes

- Part of your project points will be based on your circuit design “quality”.
- We will judge your circuit quality primarily on submitted block-diagram and state-diagram drawings of your circuits.
 - We will limit this to around 5 pages.
 - In most cases, you will not need to show details to the “gate” level.
 - Need to illustrate the major blocks, how the control and data-flow is arranged for each, and how it all fits together.
- We look for: Clarity, Simplicity, Efficiency.
- Therefore *you* need to understand your design at the circuit level – not just the Verilog level.
- **Do not use any Verilog description if you do not understand what it generates!**

Extra Credit

- Extra Credit will only be considered for working projects.
- You will only have one checkoff (either early or normal) at which time we examine standard plus extras credit.
- Extra Credit Ideas:
 - One week early checkoff 8%
 - Simultaneous display of 2 video streams 10%
 - Simultaneous display of >2 video streams 15%
 - Display of watermarks or other overlay images 8%
 - Closed captioning display 5%
 - Scaling of image using linear interpolation 8%
 - Scaling using resampling filter ($\sin(x)/x$) 15%
 - Other possible, points negotiable.
- You can receive full points for only one extra credit task, and partial points for additional ones as per the following:
Extra credit points = $\text{task}_a\text{_points} + 0.5 \text{task}_b\text{_points} + 0.25 \text{task}_c\text{_points} + \dots$