University of California at Berkeley
EECS

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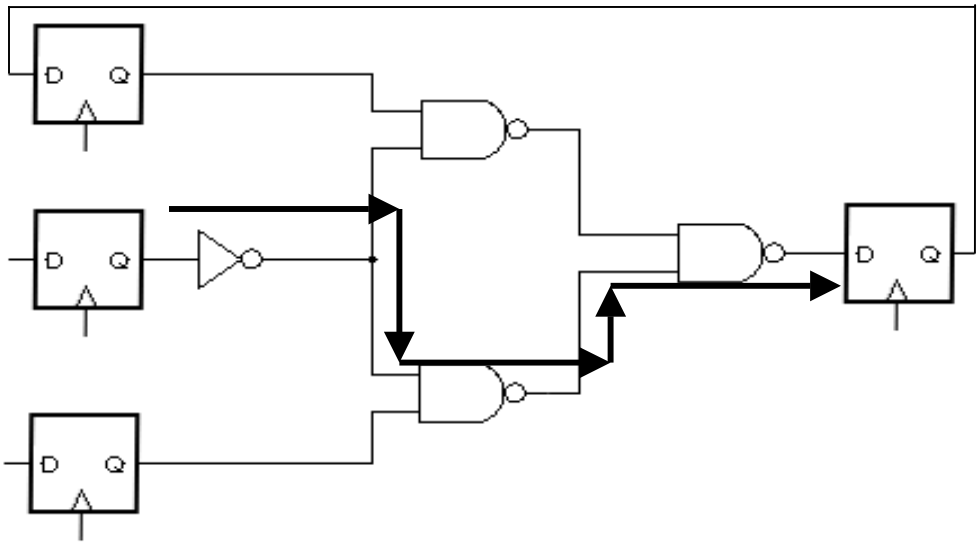
Quiz #2

Name: _____

SID: _____Lab section number: _____

For the circuit shown, assume the following:

- All transistors in the circuit are of the same strength
- For the inverter, $\tau_{HL} = \tau_{LH} = 10F$ ns where F is the # of transistors being driven.
- The degree of fanout incurred in connecting to the **D** input of a flipflop is the same as the degree of fanout incurred by connecting to an inverter.
- Setup time for a flipflop = 13 ns
- Clock-to-Q time for a flipflop = 14 + 10F ns



Given the above, answer the following questions:

1. Denote the critical path by marking it on the schematic. What is the delay associated with the critical path (excluding delay associated with the FlipFlops)?

   $10*(F_0=4)$ ns + $20*(F_1=2)$ ns + $10(F_2=2)$ ns = 100 ns
   OR
   $10*(F_0=4)$ ns + $10*(F_1=2)$ ns + $20(F_2=2)$ ns = 100 ns

2. What is the minimum clock period with which this circuit can safely be run?

   Minimum period = Clock-to-Q + CL delay + Setup time
   14ns + $10(F_0=2)$ ns + 100 ns + 13 ns = 147 ns

WHY?

- All transistors have the same strength, and, as given by the tau formula for the inverter, the delay through a gate is purely a function of fanout (i.e. a function dependent only on RC). Thus, there are 2 pull-up times and 1 pull-down time for a NAND gate, depending on input. Pulldown requires going through 2 NMOS transistors and would therefore have twice the R of the inverter. Pull-up is either going through one or both of the parallel PMOS transistors, and would therefore have either the same or half the delay of the inverter for the respective cases.
- Since the path to be determined is the critical path, only the worst case scenarios for switching must be examined.
- However, as the two NAND gates are in series, they cannot both be pulling down at the same time, as a logic low on input must produce a logic high on output. Therefore, the worst case scenario is that one NAND gate in the critical path is pulling down, and the other is pulling up, but only across one transistor. This scenario can be achieved in multiple ways, but as the fanout from each of the 3 NAND gates is the same, the order in which the gate doing the pull up and the gate doing the pull down are put doesn't affect the time for the critical path.